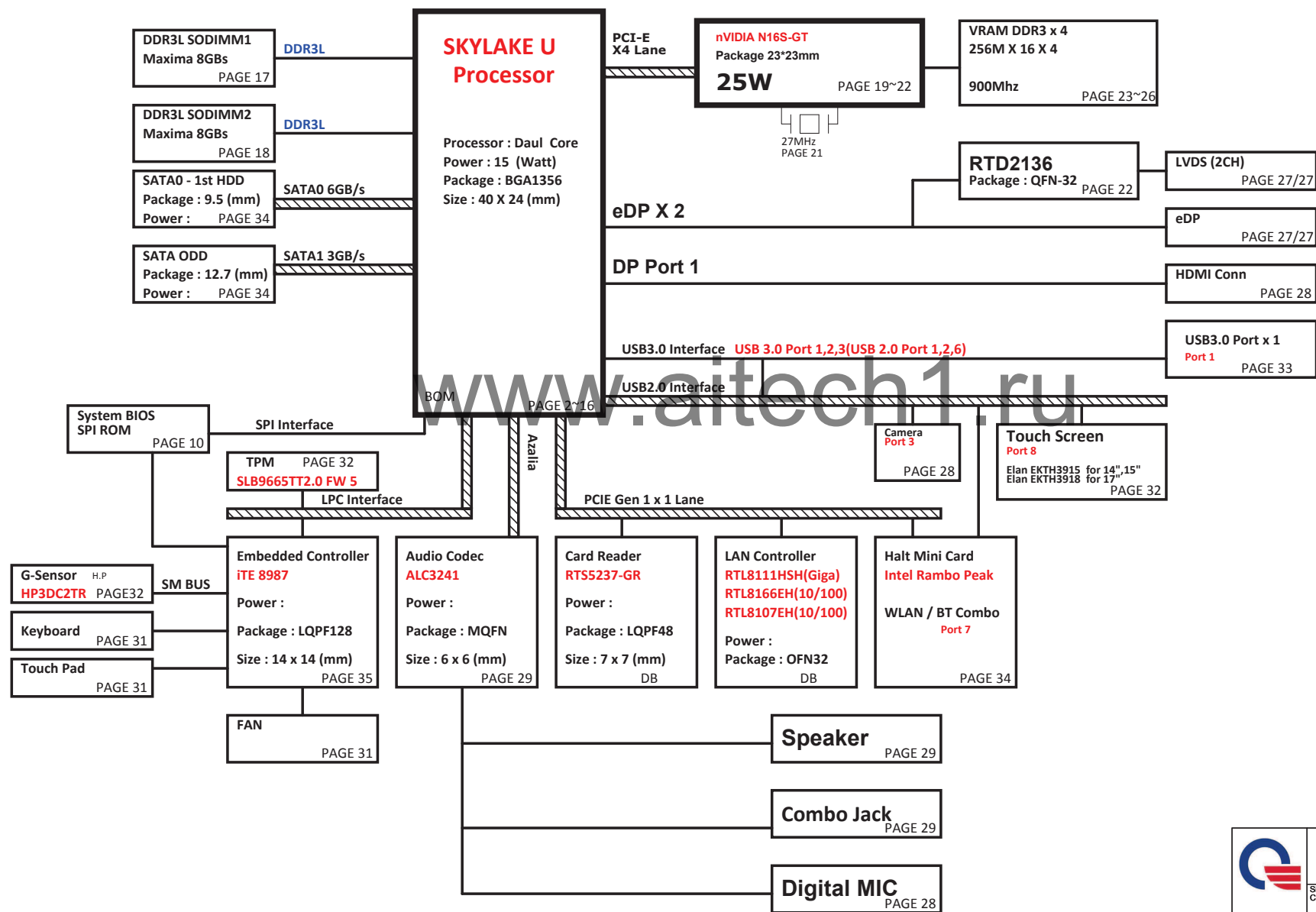


DIS (14" / 15" / 17") Chocolate

Intel SKYLAKE ULT Platform Block Diagram

PCB 6L STACK UP

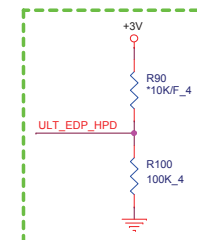
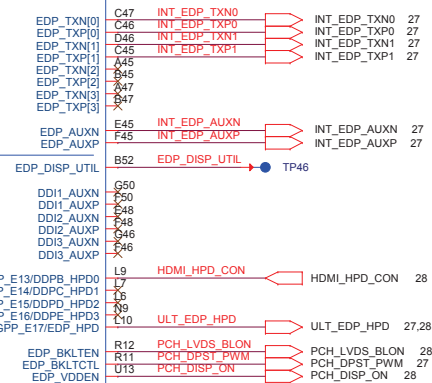
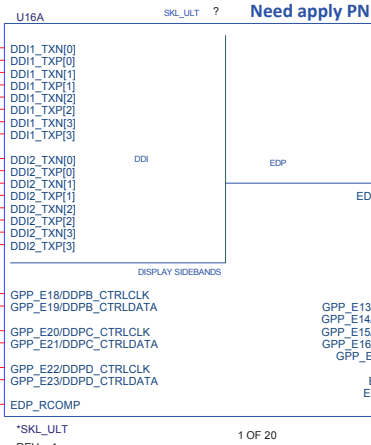
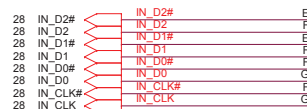
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



Reserve EDP HPD opposites circuit!

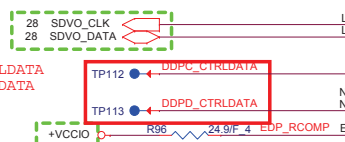
+3V 4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+1.0V 4,6,16,32,35,40
+VCCSTPLL 4,5,6,9,40,41

HDMI



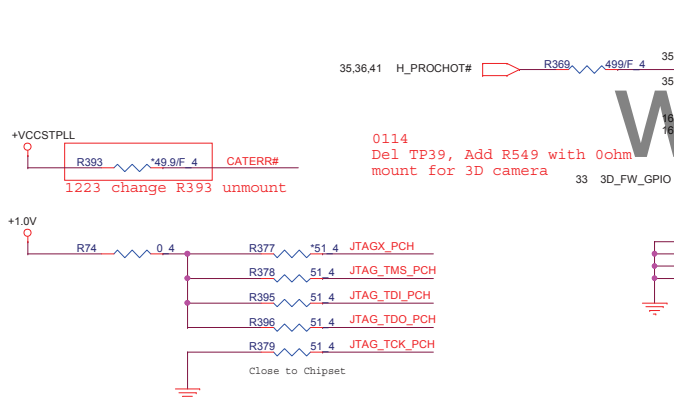
1223 Del R93, R102

1225 DDPC_CTRLDATA
and DDPC_CTRLDATA
reserve TP



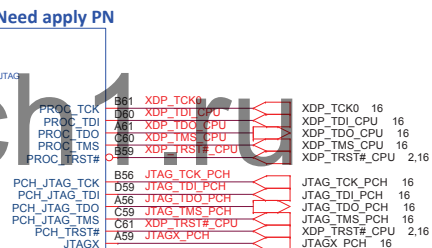
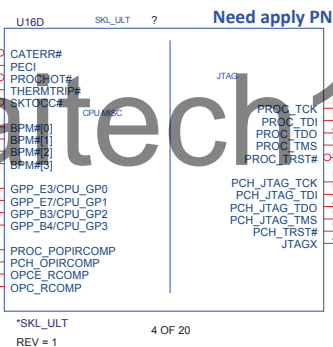
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

```
-----
1218 change R96 connection from +1.0V to +VCCIO
```



0114
Del TP39, Add R549 with 0ohm
mount for 3D camera

0305
Del tp45

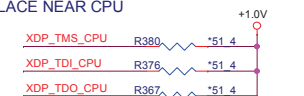


Close to EC

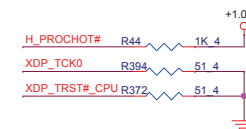


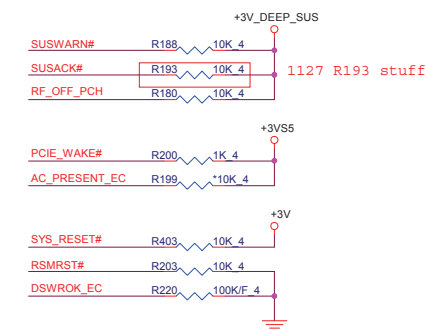
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL
470 OHM IS FOR I/P

PLACE NEAR CPU

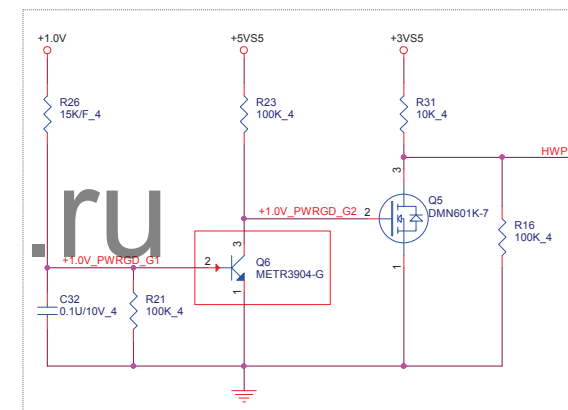
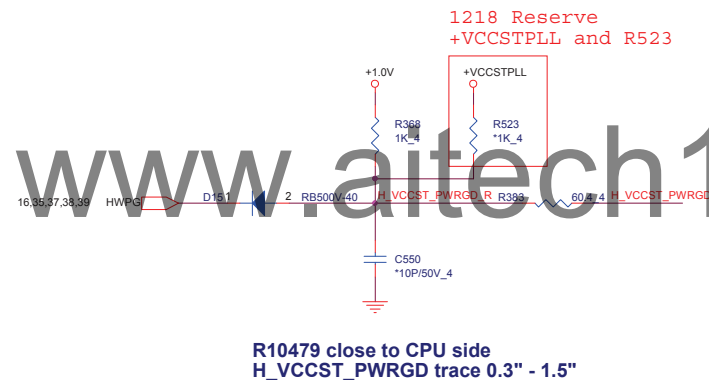
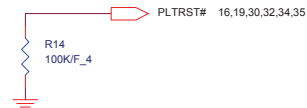


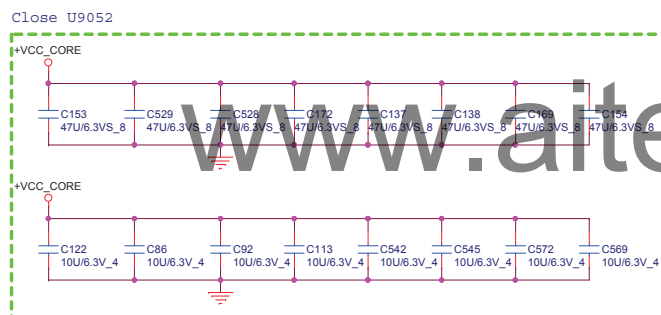
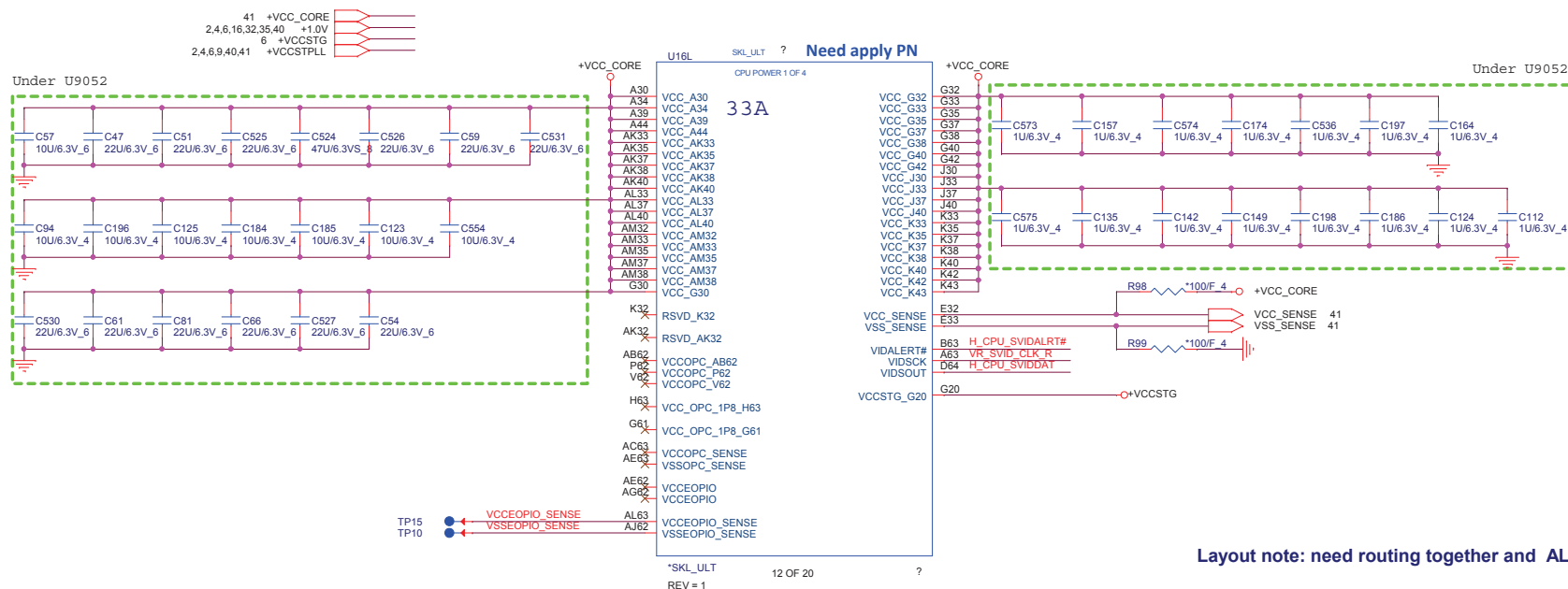
1218 Unmount R380, R367





Check Q2010 Rise/Fall time less than 100ns

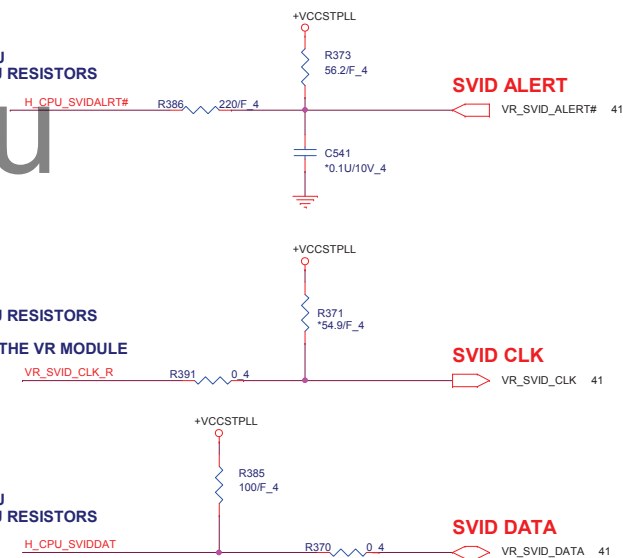




CLOSE TO CPU
PLACE THE PU RESISTORS

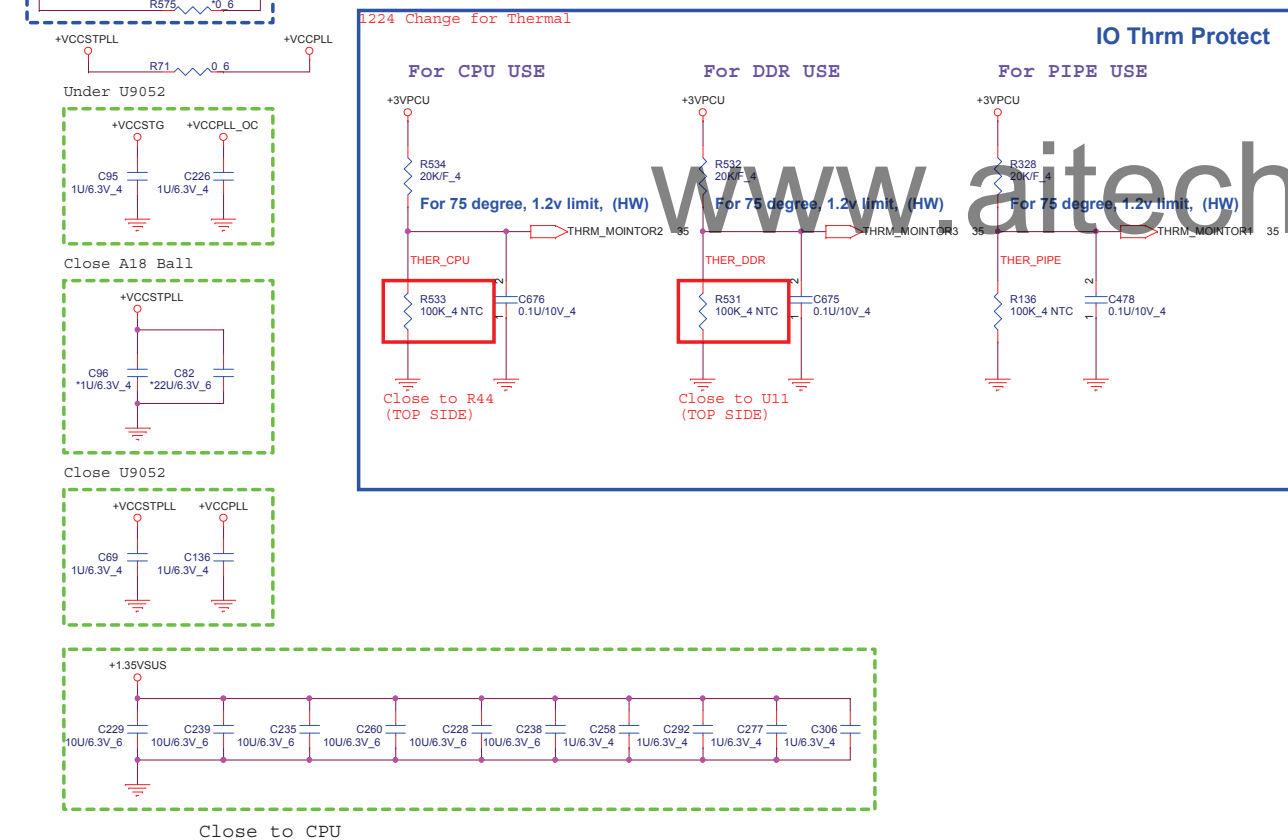
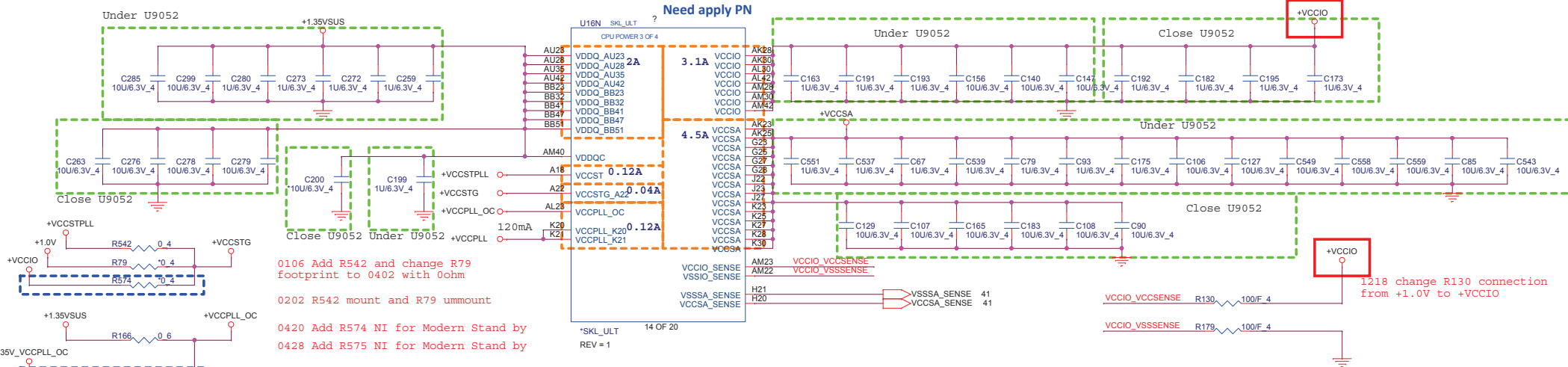
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

CLOSE TO CPU
PLACE THE PU RESISTORS



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

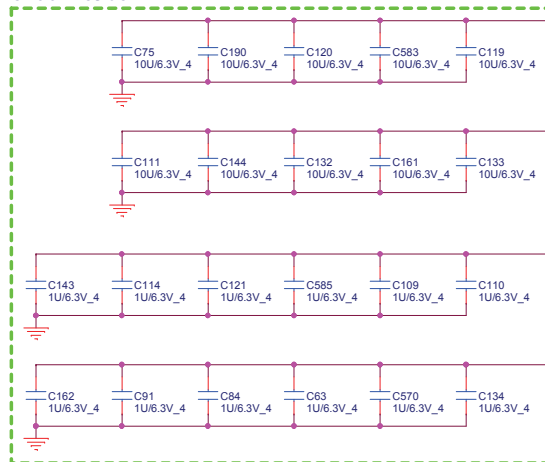
+VCCSTPLL 2,4,5,9,40,41
 +VCCSA 41,42
 +1.35VSUS 3,17,18,38,40,46
 +1.0V_DEEP_SUS 9,13,15,16,39,40
 -1.0V 2,4,16,32,35,40
 +3VPCU 13,30,31,32,33,34,35,36,37



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

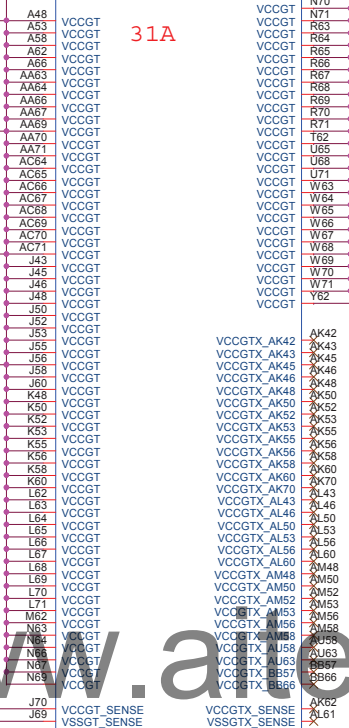
+VCCGT 41
+VCC_CORE 5,41
+1.35VSUS 3,6,17,18,38,40,46

Under U9052



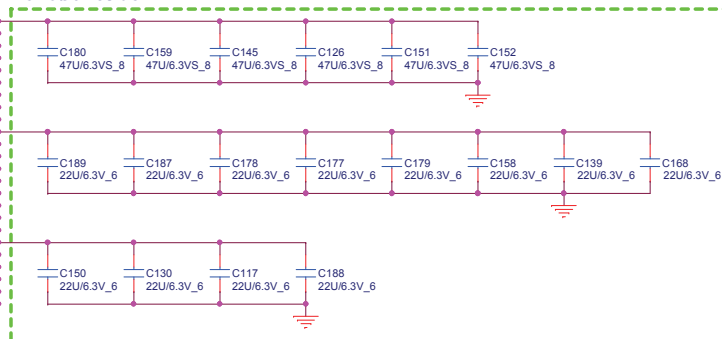
U16M SKL_ULT ? Need apply PN

31A



+VCCGT

Close U9052



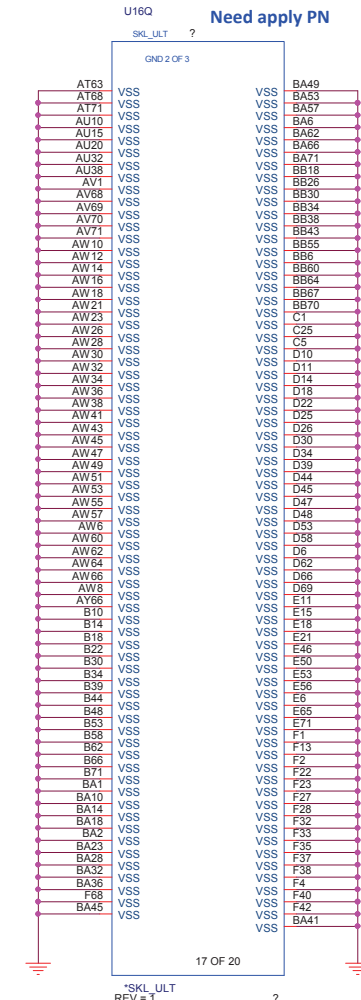
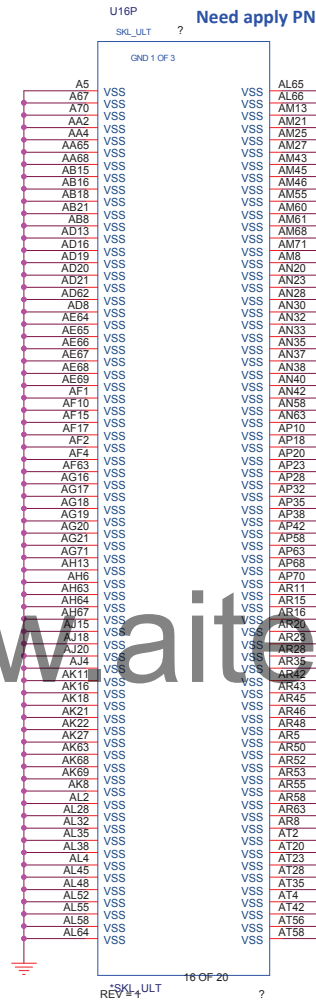
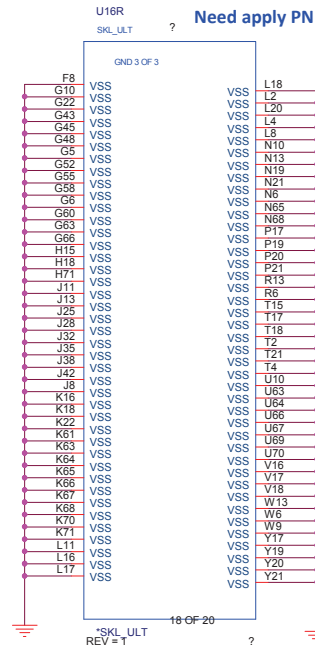
41 VCCGT_SENSE
41 VSSGT_SENSE

J70 VCCGT_SENSE
J69 VSSGT_SENSE

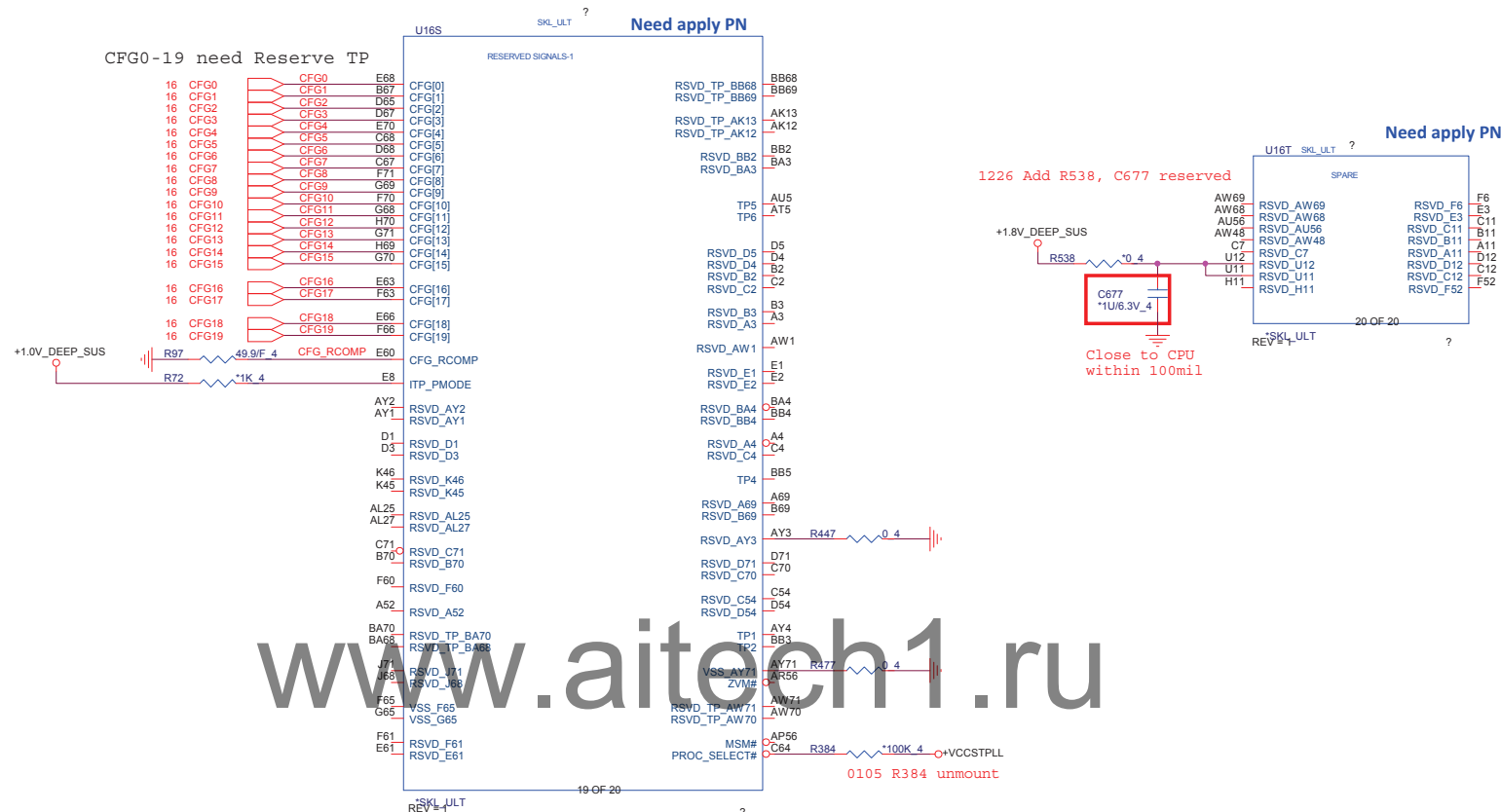
VCCGTX_SENSE
VSSGTX_SENSE

*SKL_ULT 13 OF 20
REV = 1

Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





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Processor Strapping

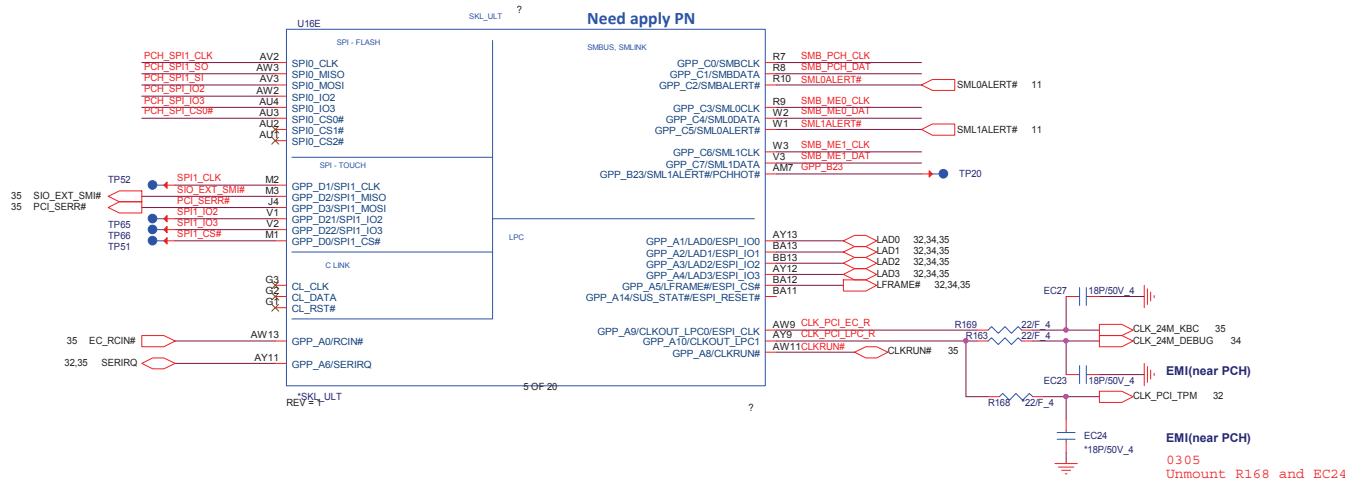
The CFG signals have a default value of '1' if not terminated on the board.

Processor Strapping			
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

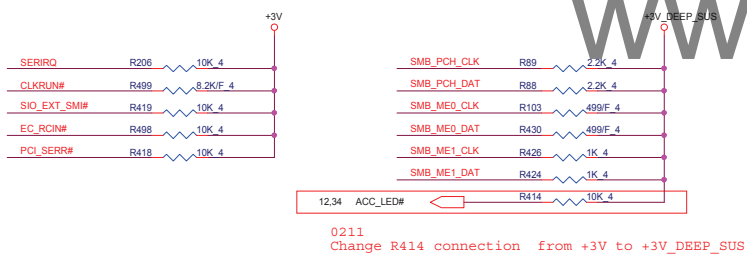


PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 9 -- SKYPAKE 12/20 (RSV-1)	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	9 of 49

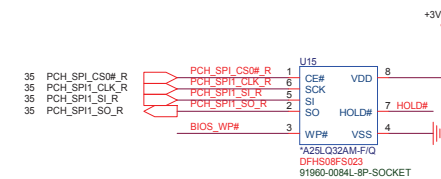


PCH SPI ROM(CLG)



Vender	Size	P/N
EON	8MB	AKE3EZNO0Q1 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFPON07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNO0Q1 (GD25B64BSIGR)
Socket		DFHS08FS023

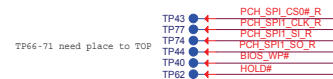
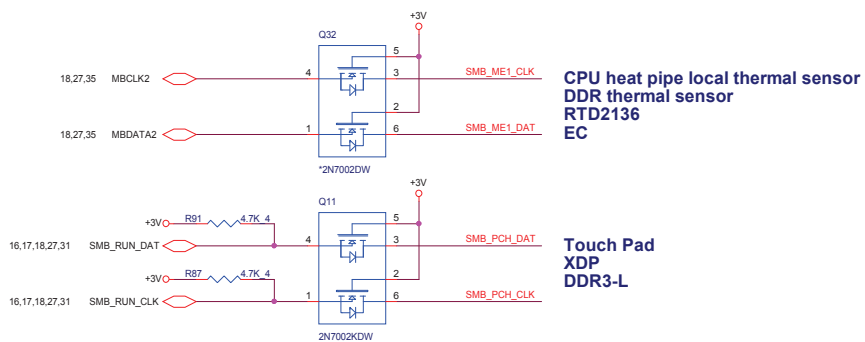
4M SPI ROM Socket



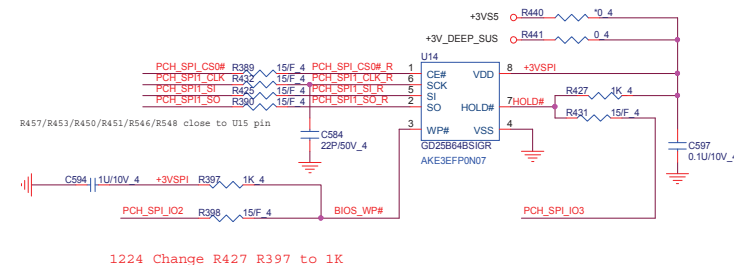
```
0211
Change mount U14, unmount U15
```

U23&U24 footprint 要重疊

SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)

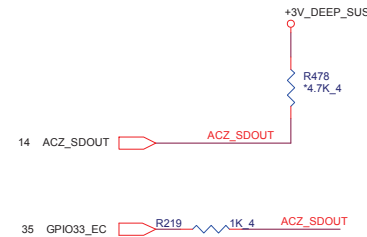
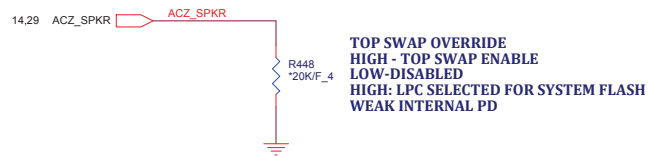


PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	Rev 1
Date: Wednesday, May 06, 2015	Sheet 10 of 49	

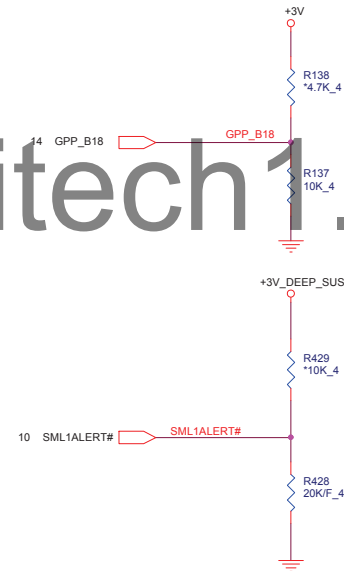
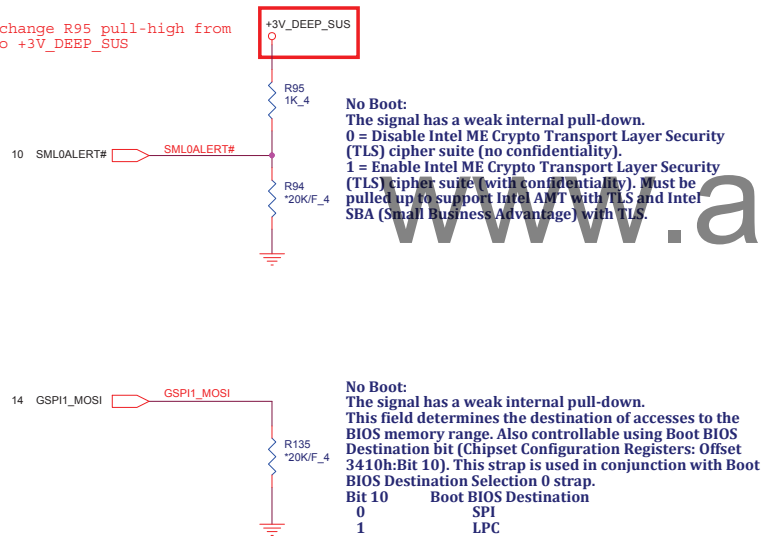
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



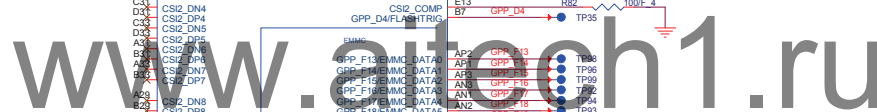
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

1212 change R95 pull-high from +3V to +3V_DEEP_SUS

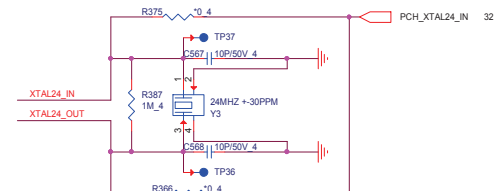



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

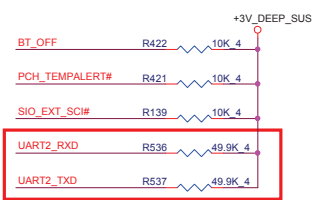


The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



	PROJECT :Y11X-6L Quanta Computer Inc.		
	Size Custom	Document Number 13 -- SKYPAKE 17/20 (CLK)	Rev 1A
Date: Wednesday, May 06, 2015		Sheet 13 of 49	

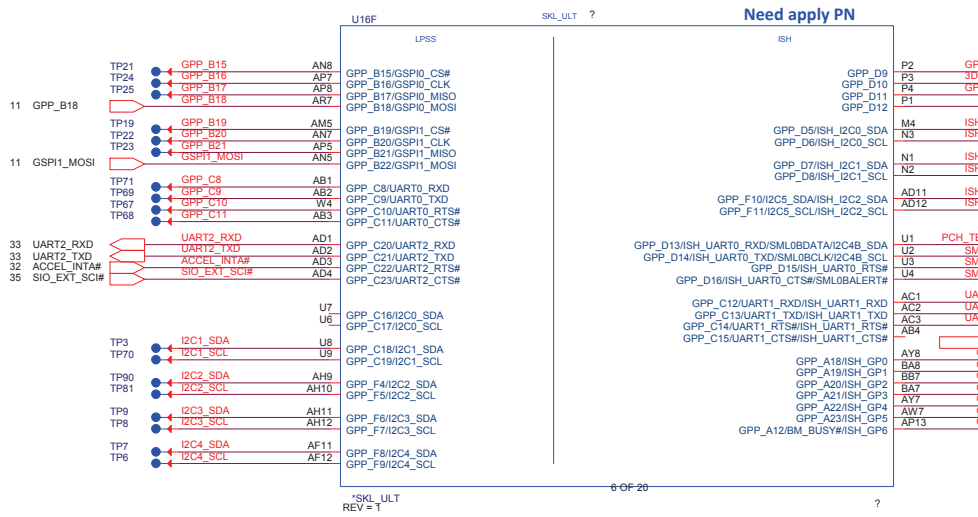
Skylake (GPIO)



1227 Add R536 and R537 for UART2 function reserved



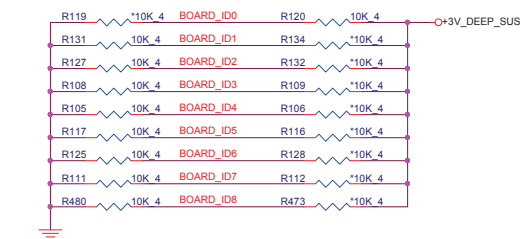
1223 Add R525



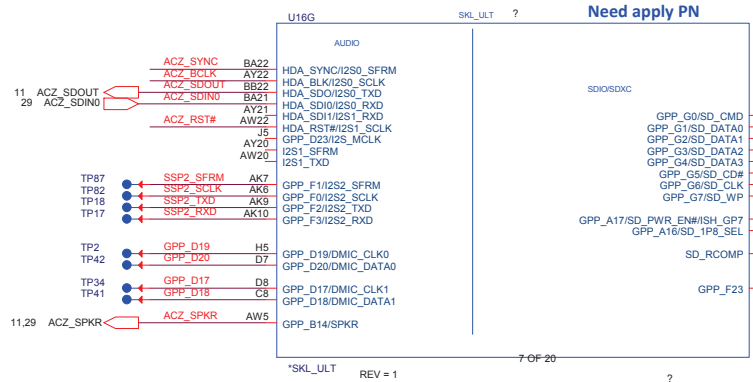
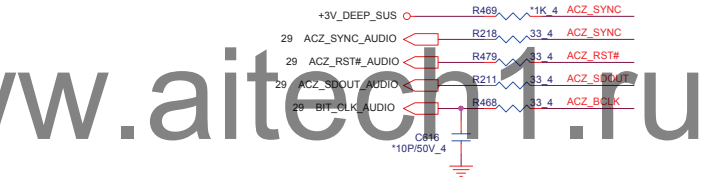
0224 Unmount R547
0114 Del TP57, Add R547 with 0ohm

0305 Del TP73

HDA Bus(CLG)



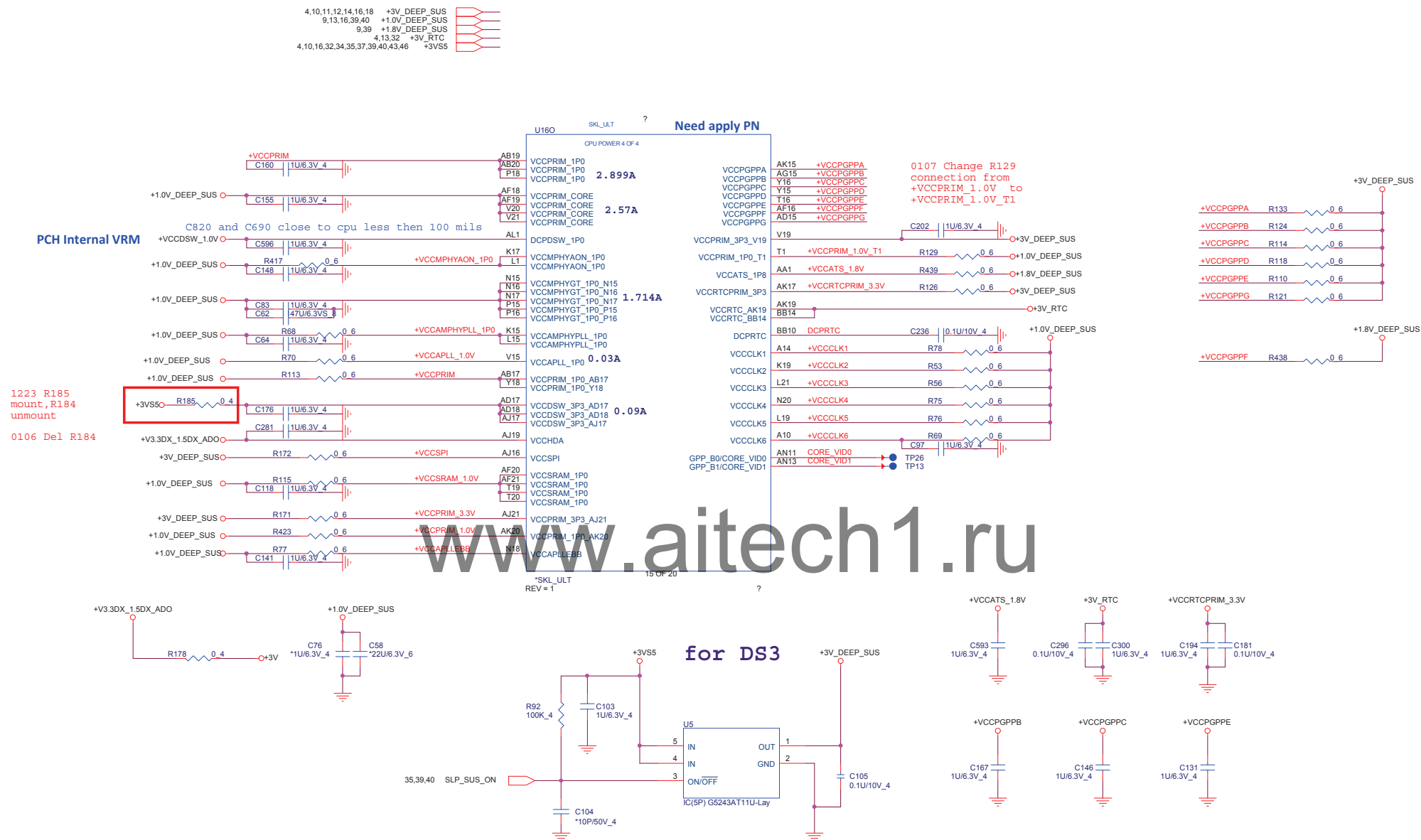
Skylake	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS



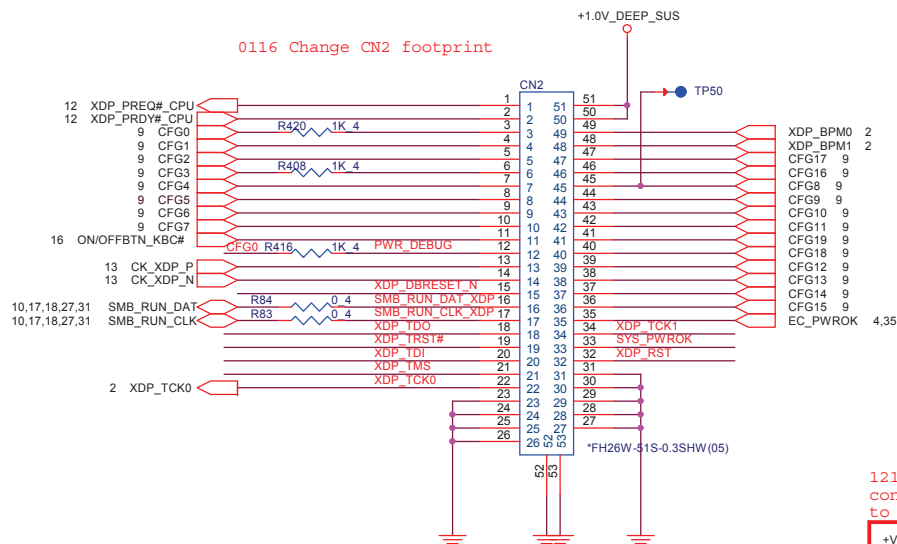
0129 Del TP110 add GPP_A16

PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 14 -- SKYPAKE 19/20 (GPIO)	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 14 of 49	

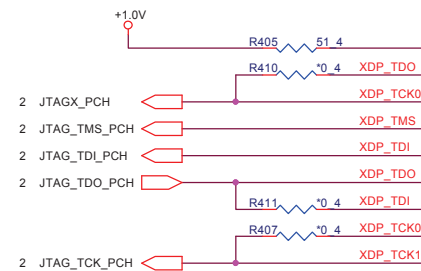
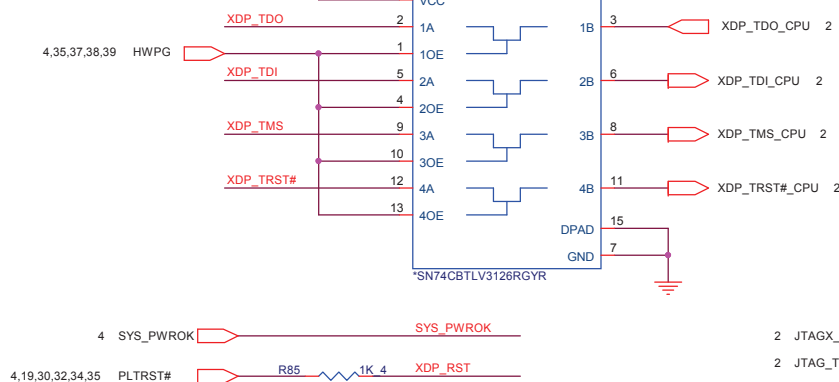
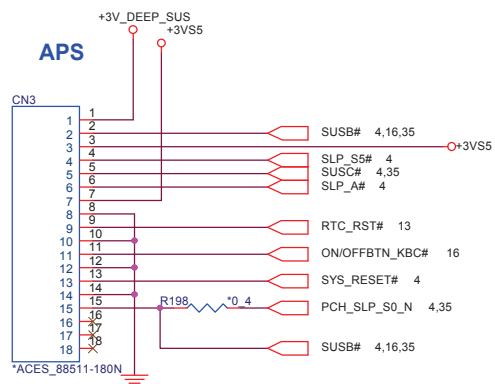


0116 Change CN2 footprint

1218 Change R86
connection from +1.0V
to +VCCIO

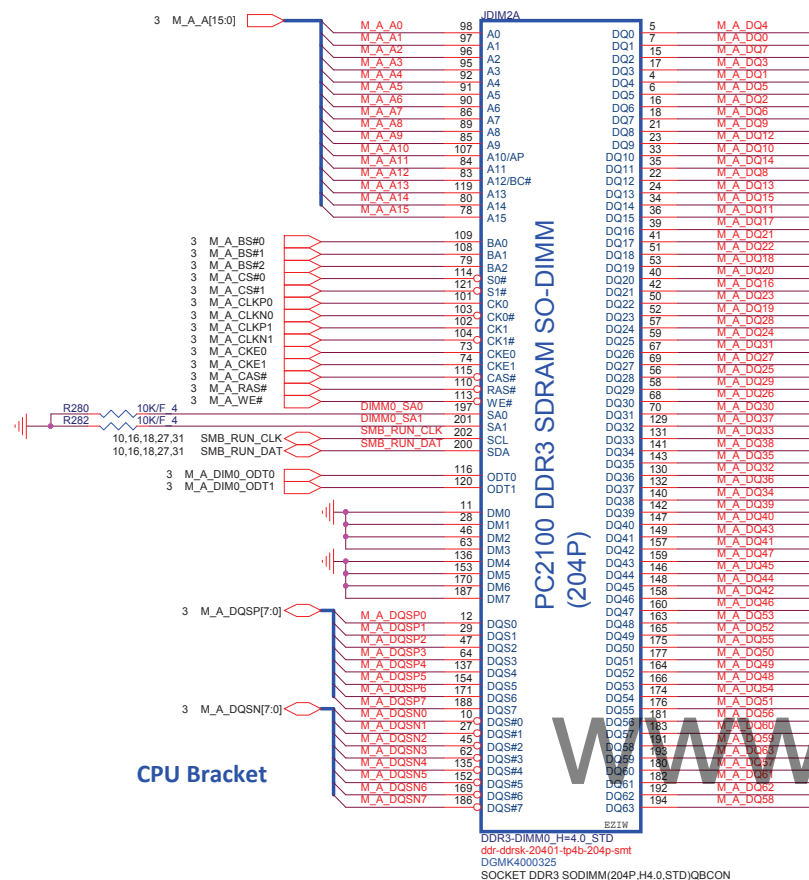
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APS



PROJECT :Y11X-6L
Quanta Computer Inc.

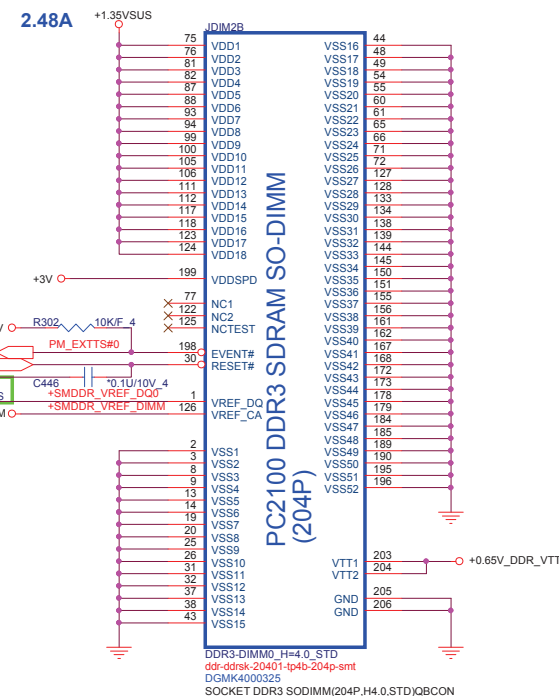
Size	Document Number	Rev
	16 -- HSW XDP & APS	1A
Date: Wednesday, May 06, 2015	Sheet 16 of 49	



CPU Bracket

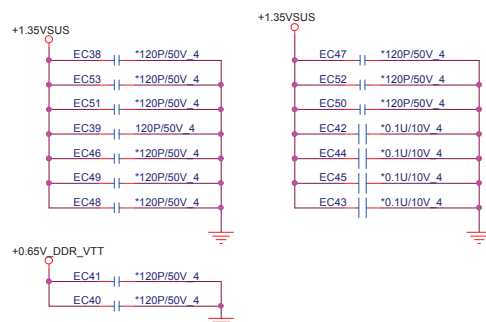
M_A_DQ[63:0] 3

PV modify to short pad



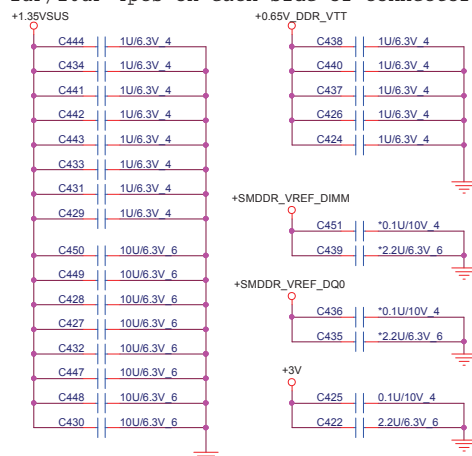
2,4,10,11,12,13,14,15,16,18,20,27,28,29,30,31,32,33,34,35,41,43,44 +3V
3,6,18,38,40,46 +1.35VSUS
18,38 +0.65V_DDR_VTT
18 +SMDDR_VREF_DIMM

For EMI RESERVE

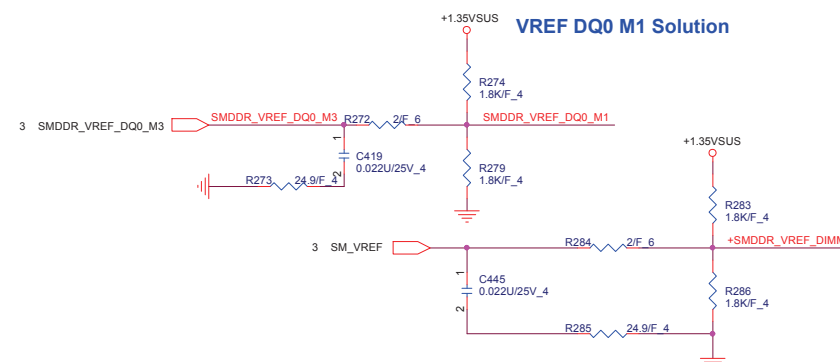


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



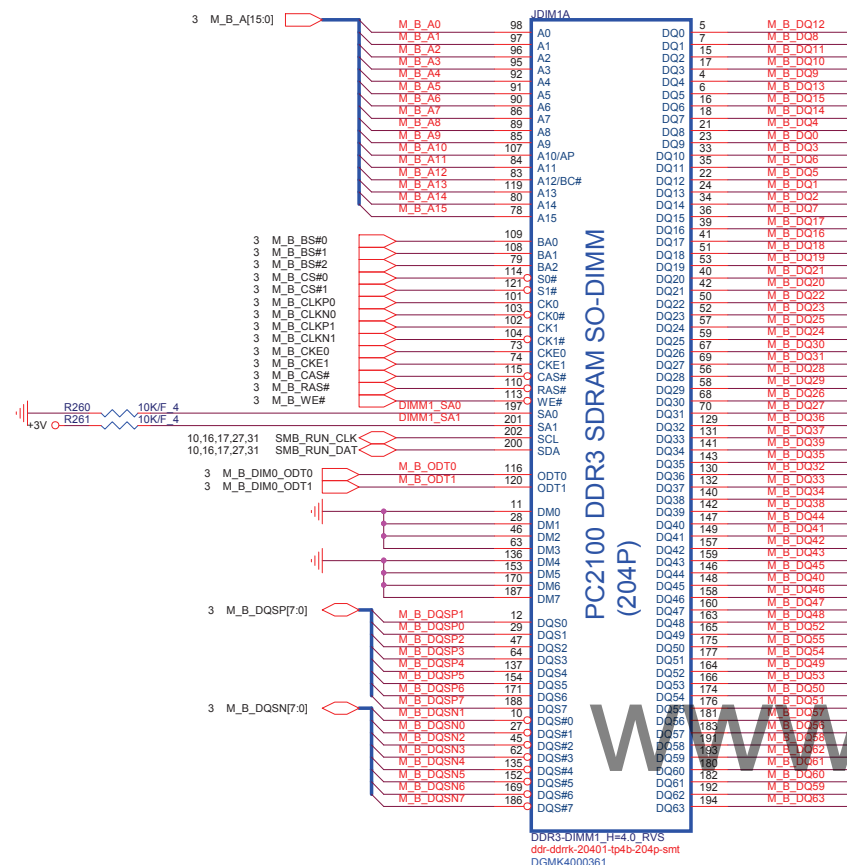
VREF DQ0 M1 Solution



PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 17 - DDR3 DIMM0-STD(4.0H)	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	17 of 49

M_B_DQ[63:0] 3




```
1230 Change C587
size to 0603
```

$$\text{PEX IOVDD} + \text{PEX IOVDDQ} = 1.042\text{A}$$

PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA

NVDD = 32.22 ~ 26.66 A +VGACORE

VDD33 = 56mA

C243	4.7U/6.3V_6	Near GPU
C247	1U/6.3V_4	

1230 Change C247,
C294 size to 0402

Power up sequence

Power down sequence

ALL 3.3V
+3VGFX & +3V3 AON

NVVDD
+VGACORE

PEX_VDD
+1.05V GFX

FBVDDQ
+1.35V GFX

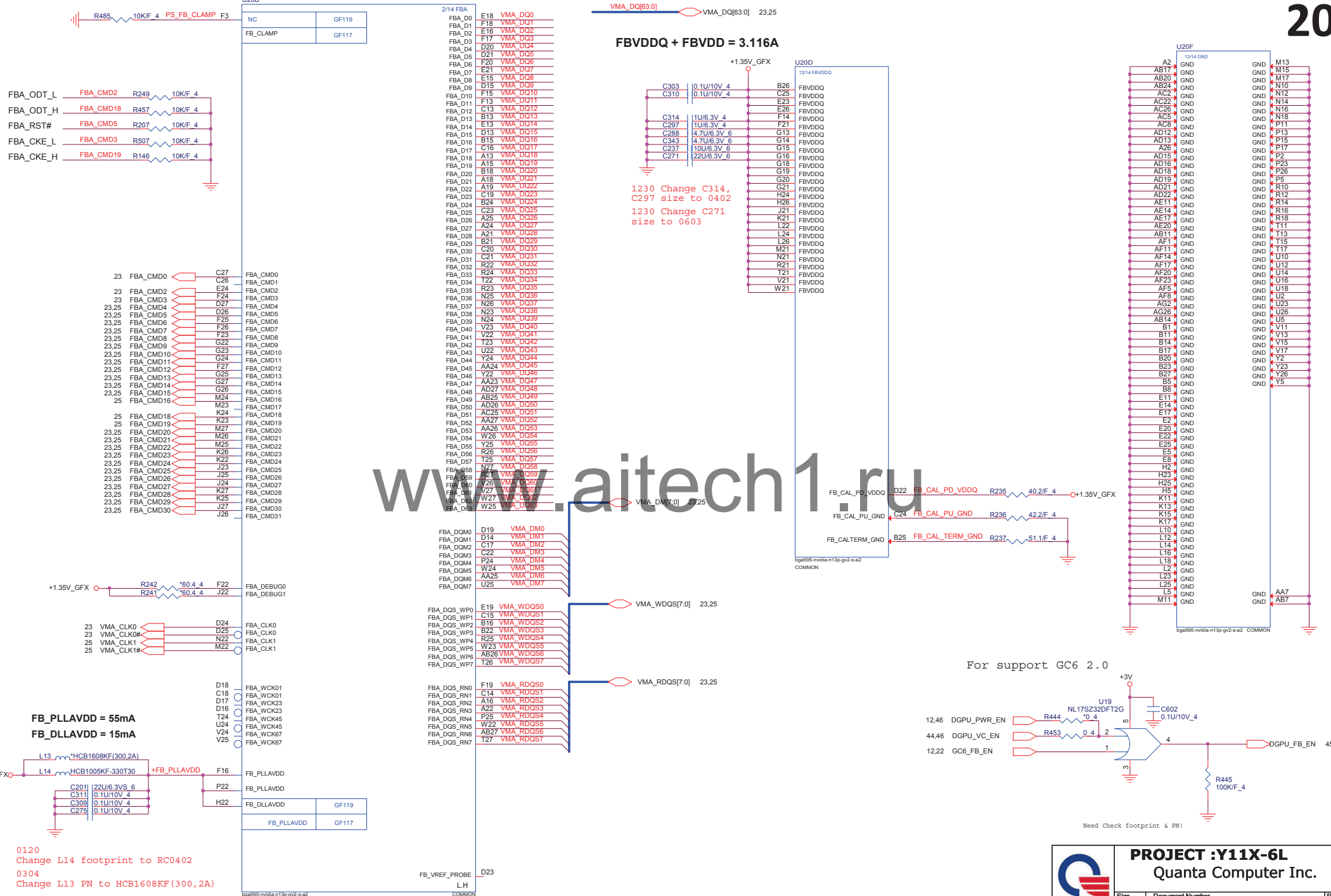
First Rail to Power

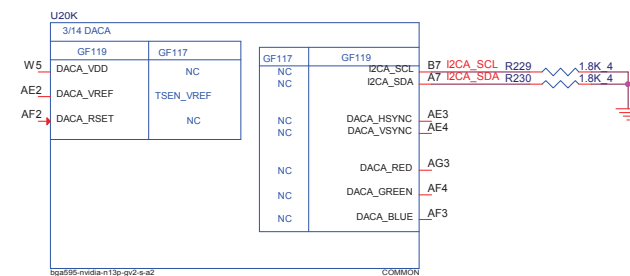
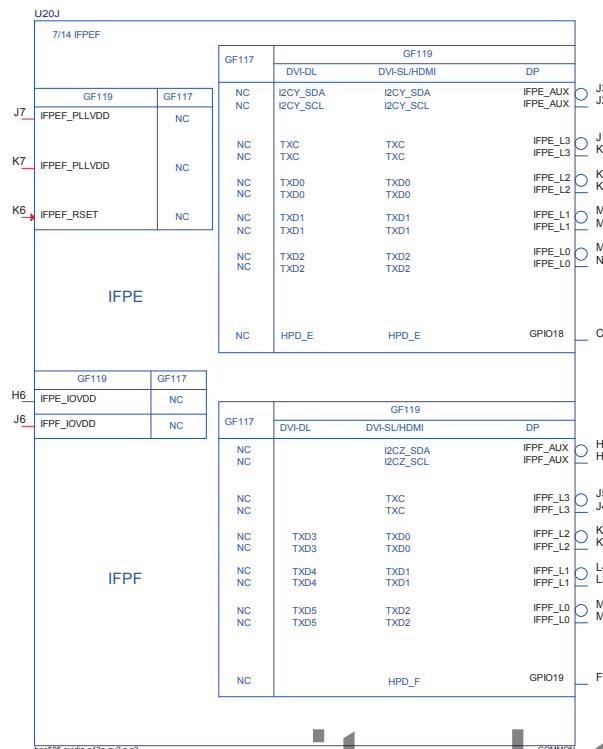
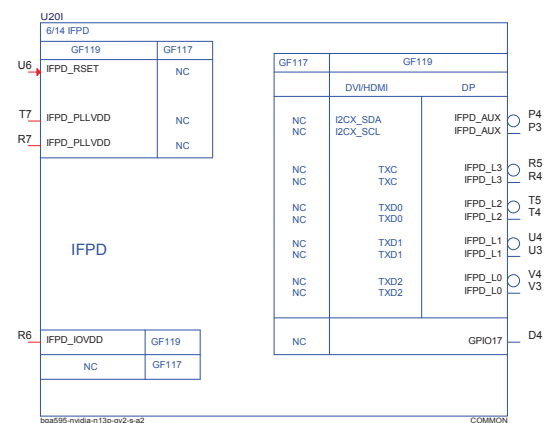
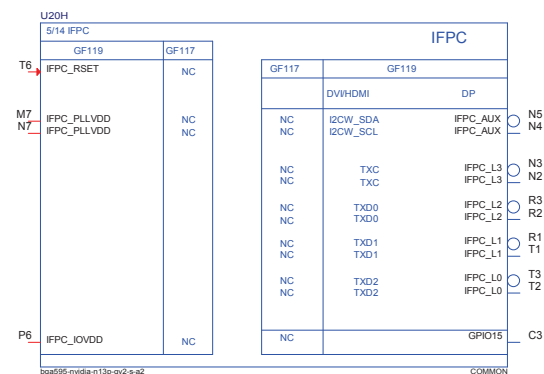
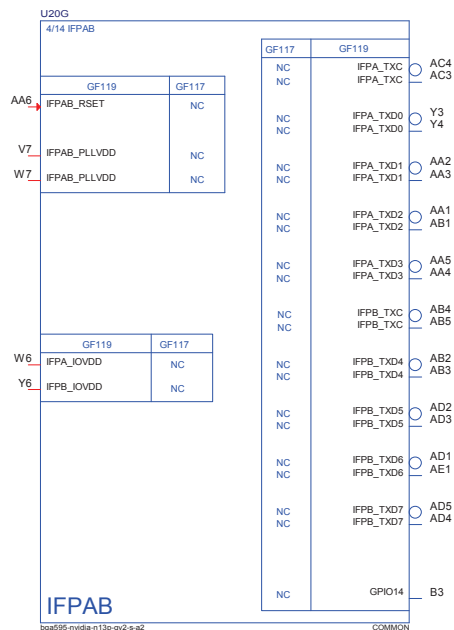
Last Rail to Power



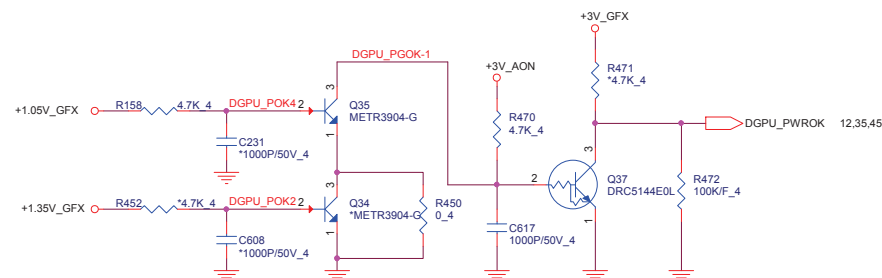
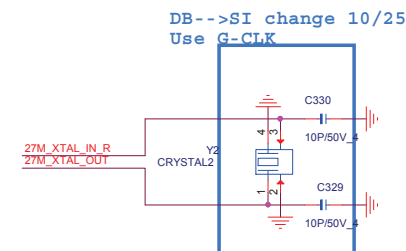
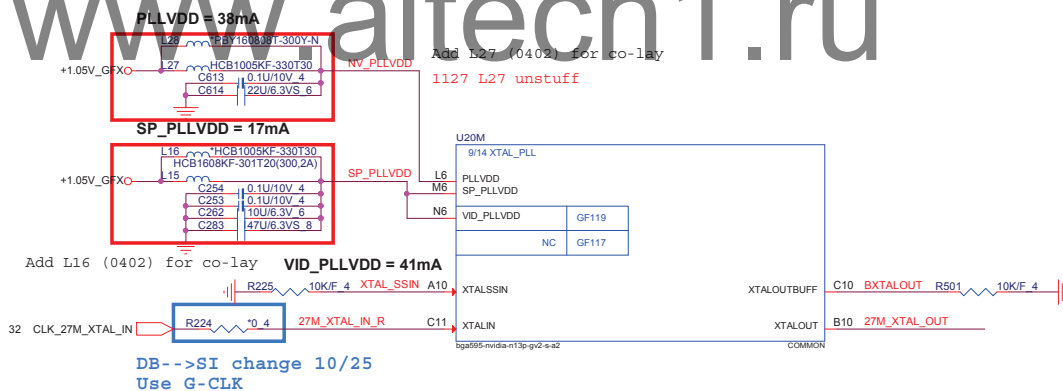
PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 19 – N15S-GT (PCIE I/F) /NVDD	Rev 1A
Date: Wednesday, May 06, 2015		Sheet 19 of 49





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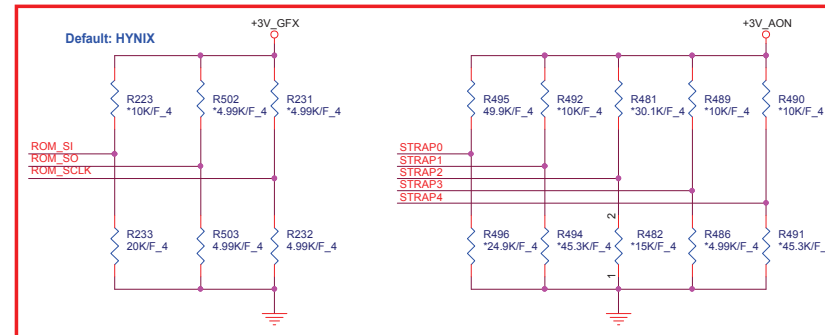
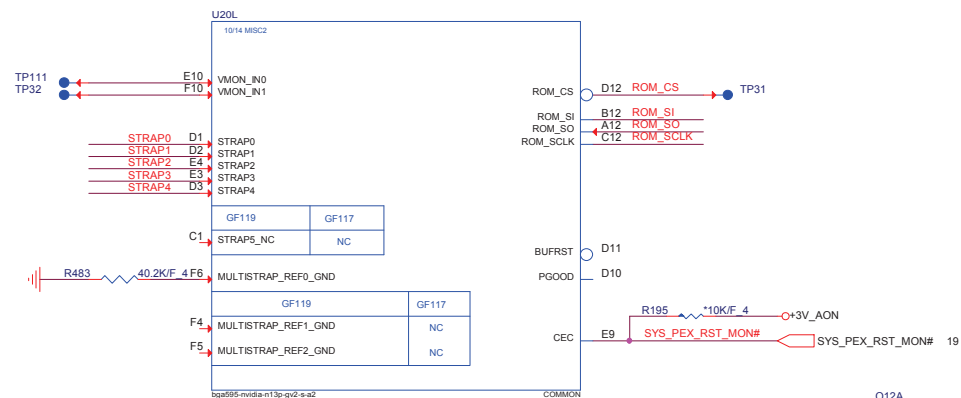
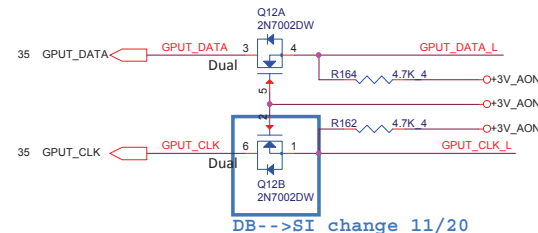
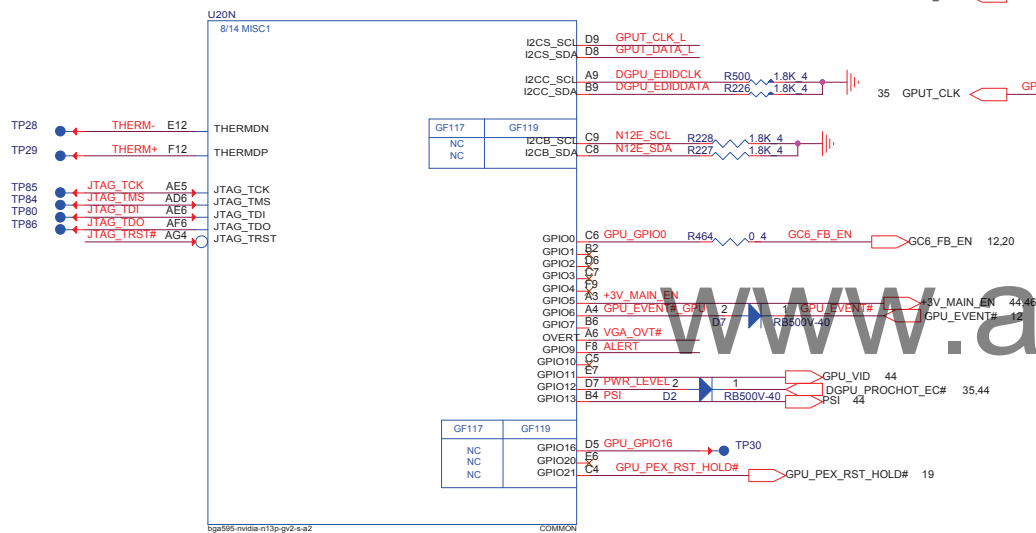


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3L 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC4G63CFR-N0C	0x2	AKD5PZDWTW01	AKD5PZDWTW02
0010	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16HA-093G:E	0x4	AKD5PZSTL00	AKD5PZSTL01
0100	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x1	AKD5PGDT500	AKD5PGDT501
0001	DDR3L 256Mx16, 64bit, 4Gb,900MHz					

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



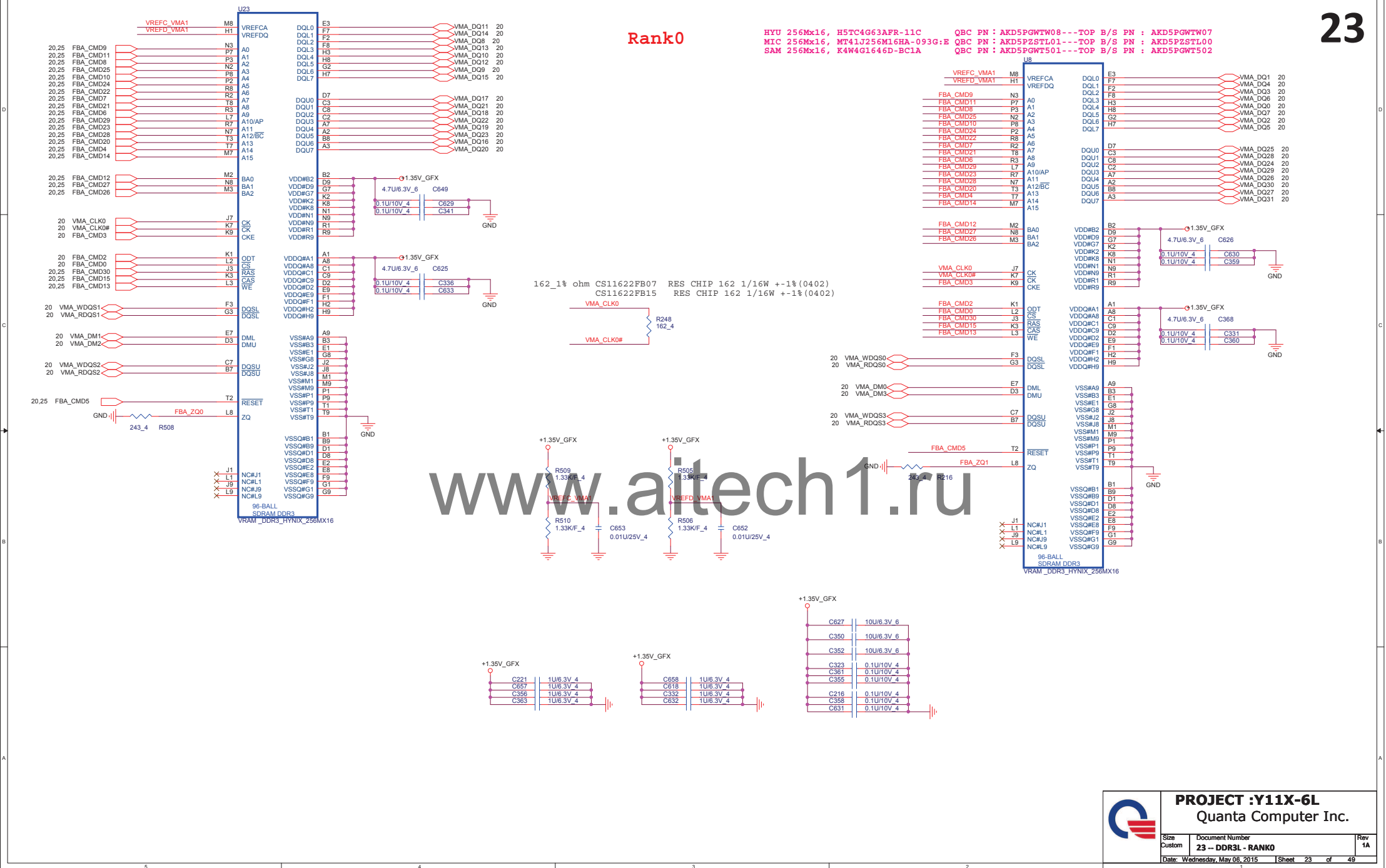
PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	22 - N15S-GT (GPIO/STRAPS)	1A
Date: Wednesday, May 06, 2015	Sheet 22 of 49	


Rank0

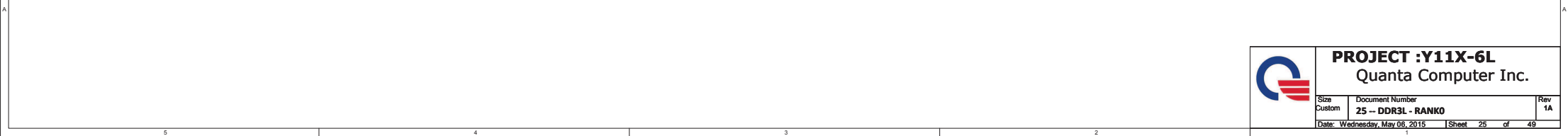
HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502




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			PROJECT :Y11X-6L Quanta Computer Inc.		
Size Custom	Document Number 24 -- Reserve				Rev 1A
Date: Wednesday, May 06, 2015			1	Sheet 24 of 49	

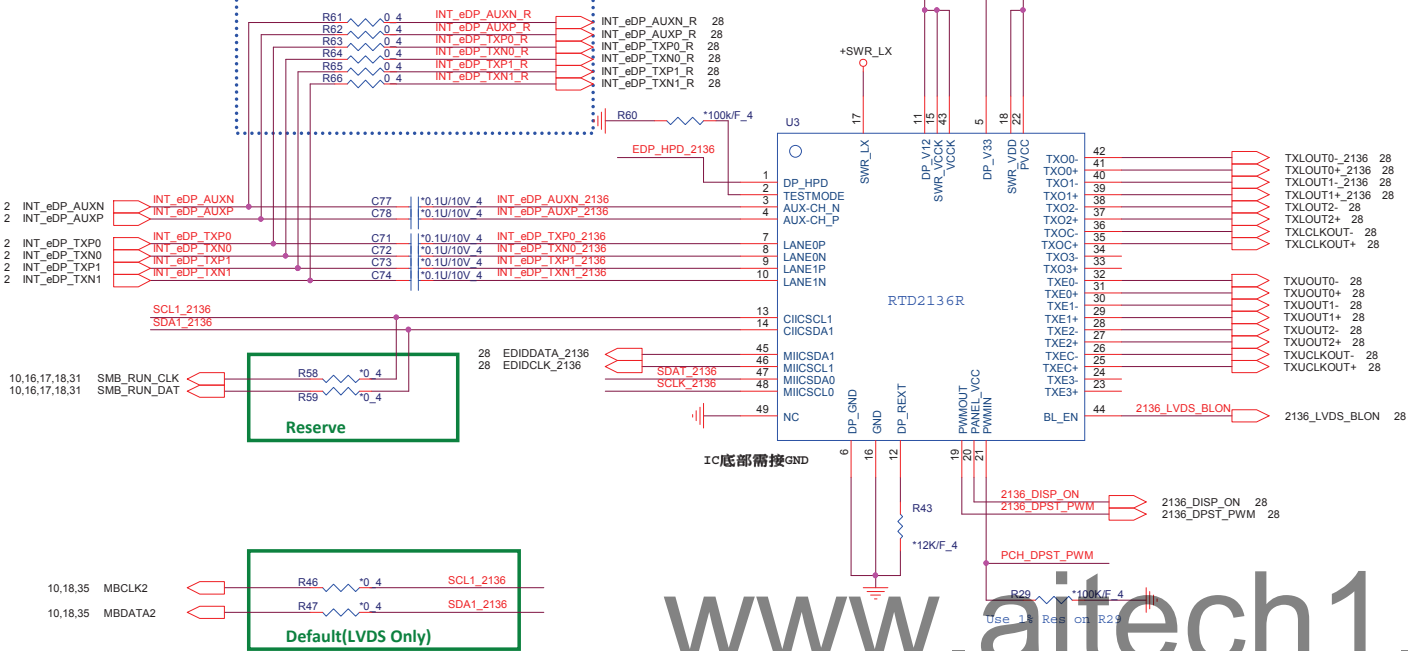


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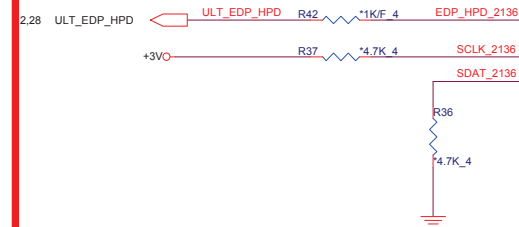
			PROJECT :Y11X-6L Quanta Computer Inc.		
Size Custom	Document Number 26 -- Reserve				Rev 1A
Date: Wednesday, May 06, 2015			Sheet	26	of 49


RTD2136 Dual Channel only

Pin 18: keep 80mil Trace

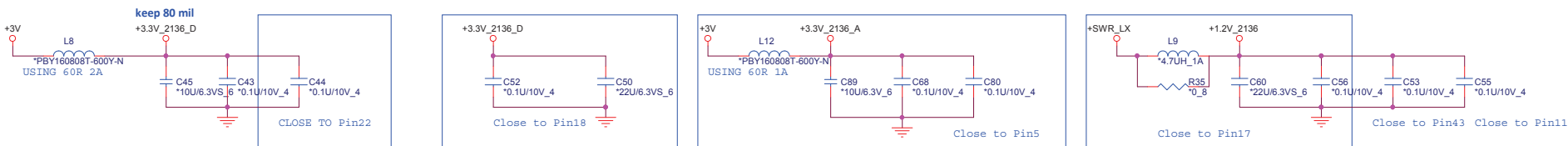


LVDS Only



2,4,10,11,12,13,14,15,16,17,18,20,28,29,30,31,32,33,34,35,41,43,44 +3V 

L9: need use CV-4709MN00 for Vendor suggestion



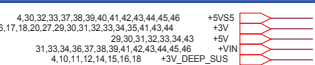
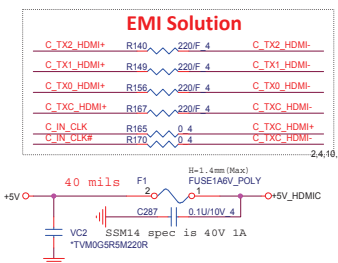
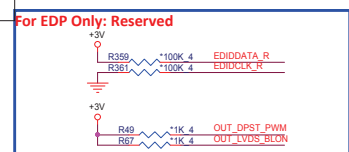
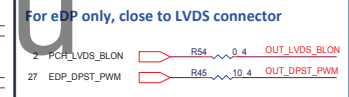
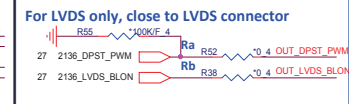
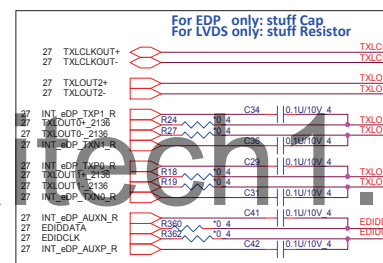
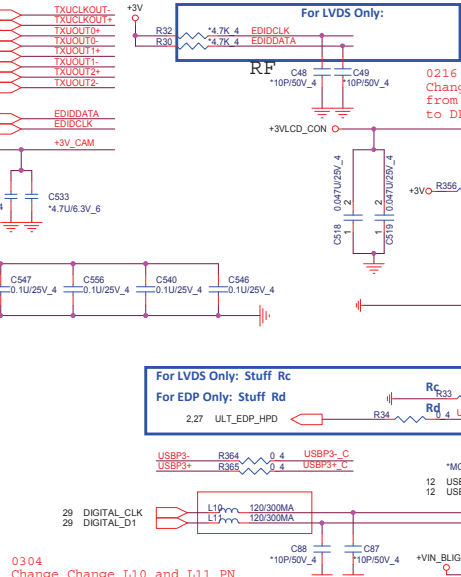
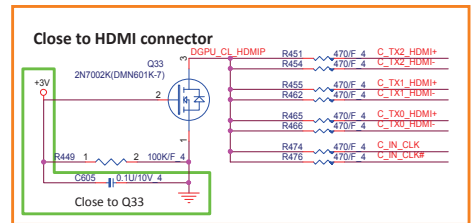
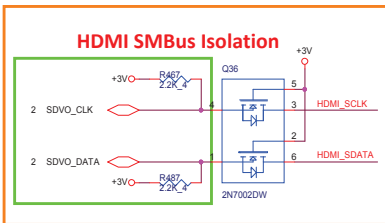
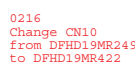
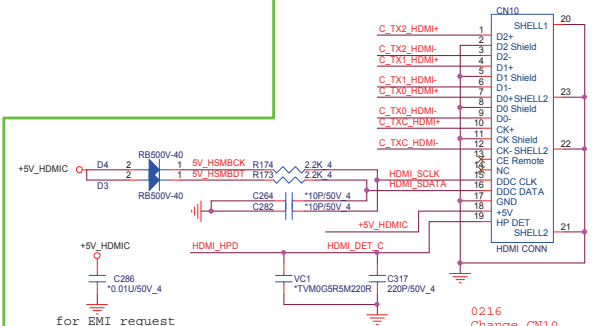
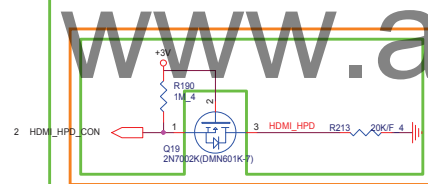
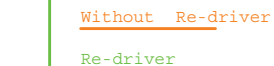
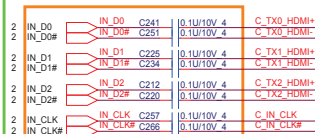
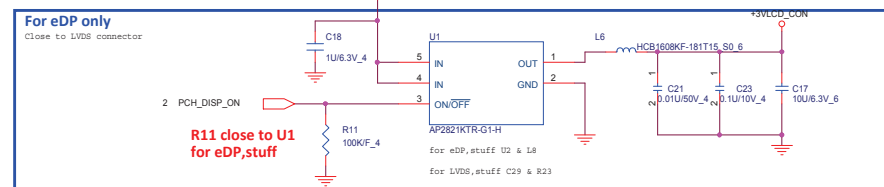
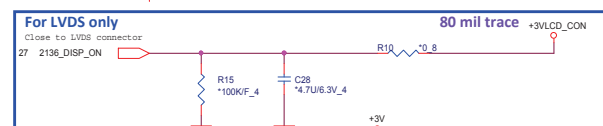
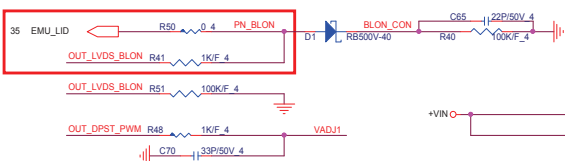
SWR MODE	LDO MODE
Stuff L9	Stuff R35

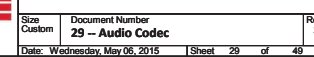


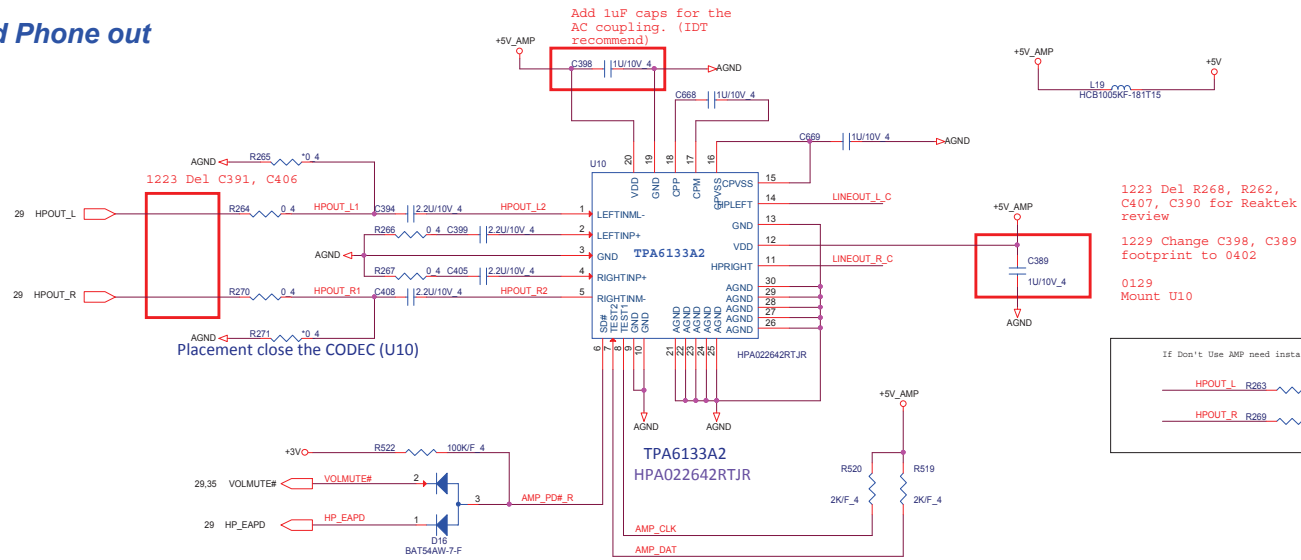
PROJECT :Y11X-6L
Quanta Computer Inc.

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LID Switch

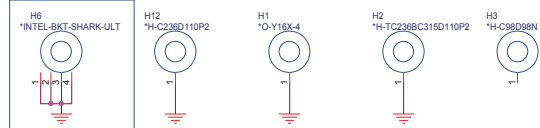




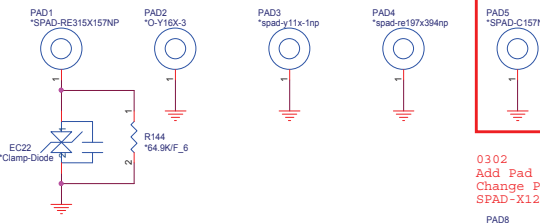
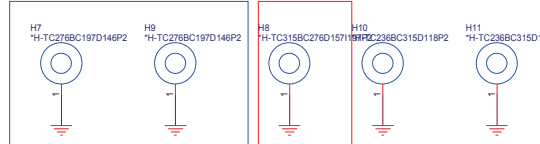


HOLE

CPU



GPU



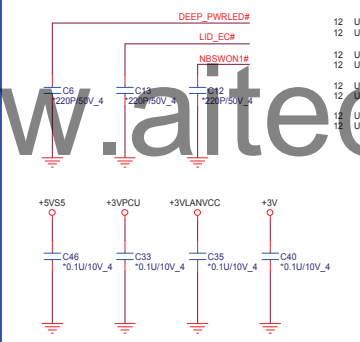
0206 Change H4 footprint from
H-C315D157P2 to
H-C315D157I197P2

0206 Change H8 footprint from
H-TC315BC276D157P2 to
H-TC315BC276D157I197P2

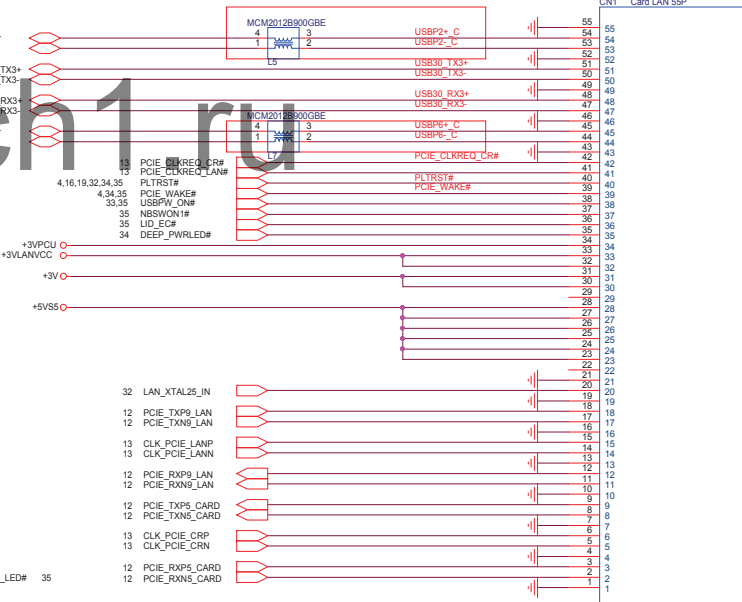
0105 Add Pad for 1229 DXF

0302 Add Pad for 0216 DXF
Change Pad7 footprint from
SPAD-X12-12NP to SPAD-X1AD-2NP

USB/CR/LAN board CONN

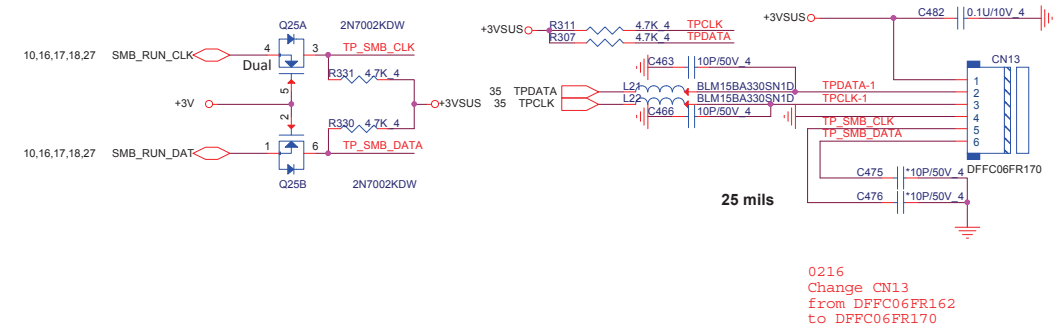


0304 Mount L5 and L7
Change Net name after L5 and L7

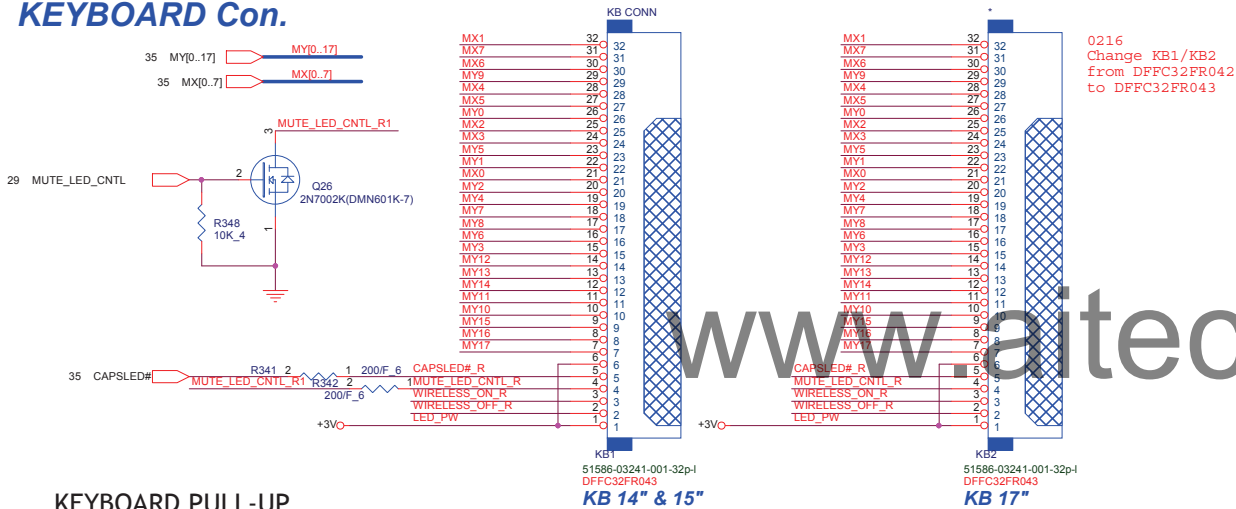


PROJECT :Y11X-6L
Quanta Computer Inc.

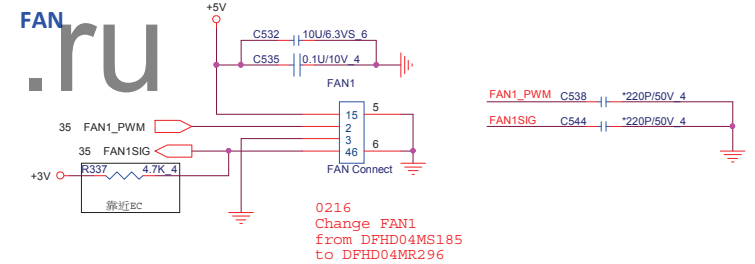
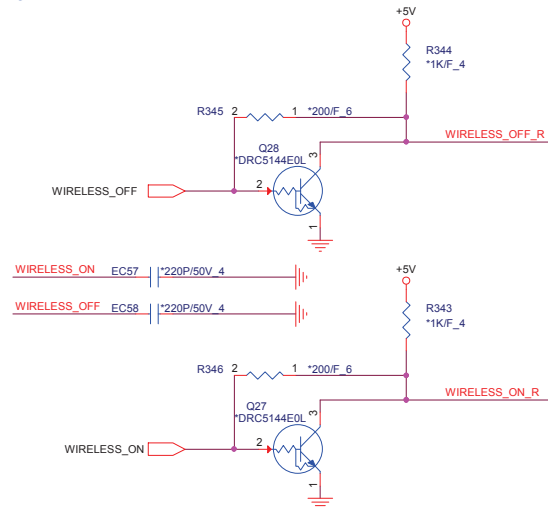
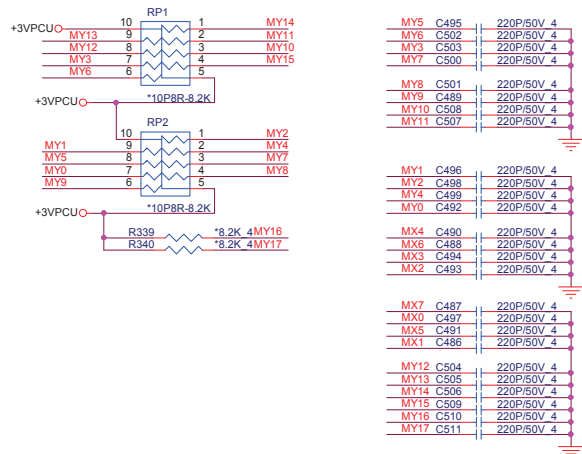
Size C Document Number 30 - Card Reader Rev 1A
Date: Wednesday, May 06, 2015 Sheet 30 of 49



KEYBOARD Con.



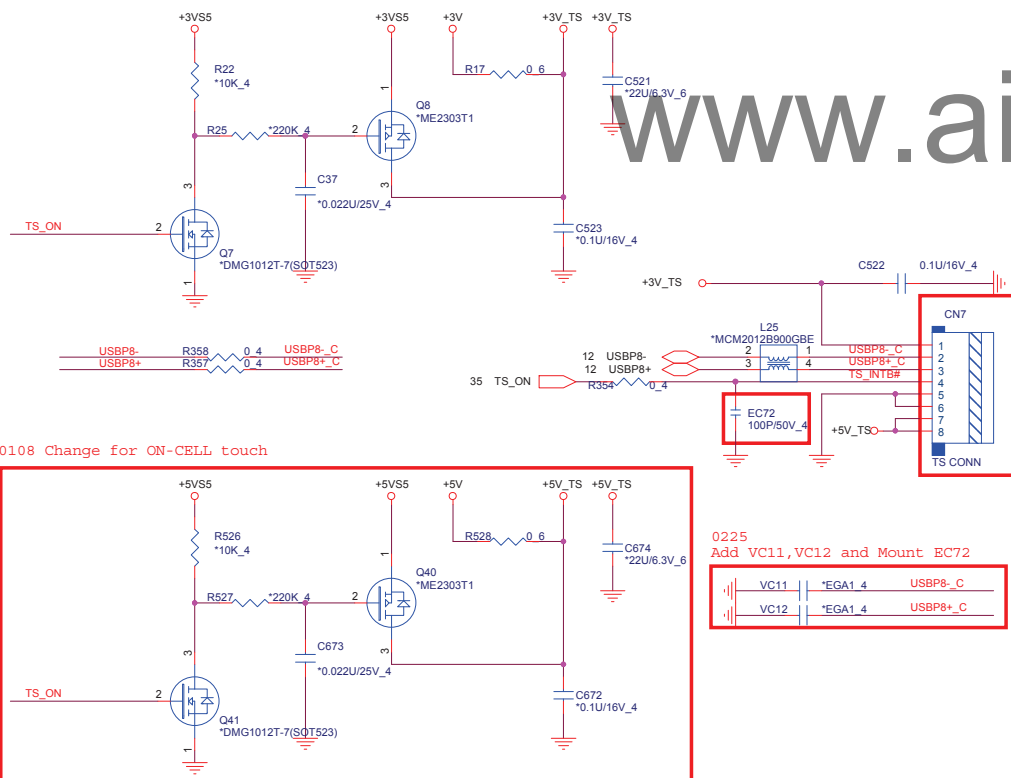
KEYBOARD PULL-UP



	BADD
HIGH	4EH/4F

+3V

FOR EMI



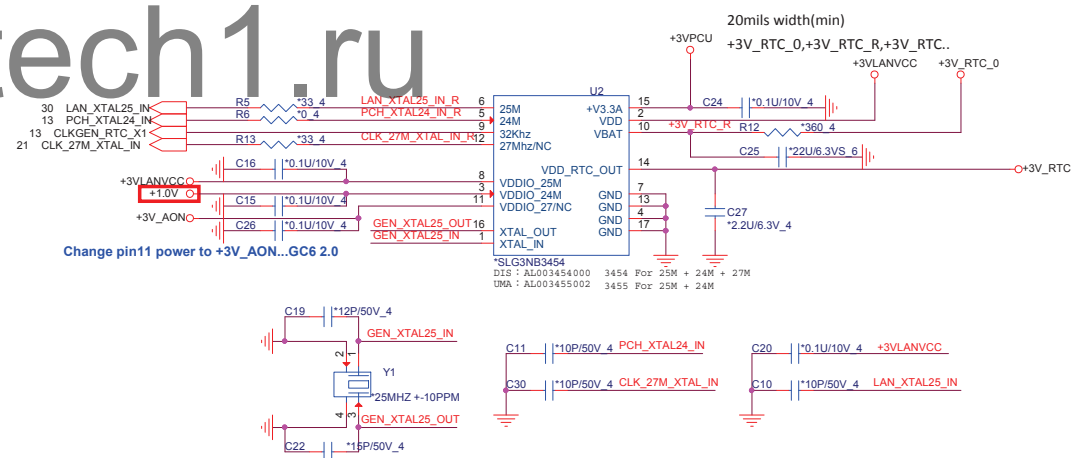
32

The schematic diagram illustrates the connection between the HP3DC2TR module (U7) and the AL003DC2A00 module. The HP3DC2TR module is a 14-pin component with pins 1, 14, 2, 3, 10, 13, 15, 16, 5, and 12. The AL003DC2A00 module is a 14-pin component with pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14. The connections are as follows:

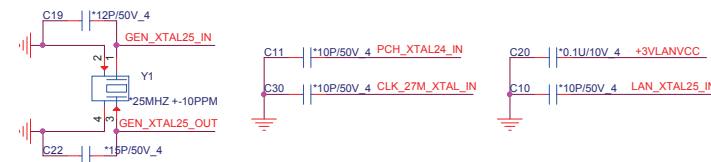
- Pin 1 (HP3DC2TR) to Pin 14 (AL003DC2A00):** Vdd_IO
- Pin 14 (HP3DC2TR) to Pin 1 (AL003DC2A00):** VDD
- Pin 2 (HP3DC2TR) to Pin 10 (AL003DC2A00):** NC
- Pin 3 (HP3DC2TR) to Pin 13 (AL003DC2A00):** NC
- Pin 10 (HP3DC2TR) to Pin 15 (AL003DC2A00):** NC
- Pin 13 (HP3DC2TR) to Pin 16 (AL003DC2A00):** NC
- Pin 5 (HP3DC2TR) to Pin 12 (AL003DC2A00):** GND
- Pin 12 (HP3DC2TR) to Pin 5 (AL003DC2A00):** GND
- Pin 1 (AL003DC2A00) to Pin 11 (HP3DC2TR):** INT1
- Pin 2 (AL003DC2A00) to Pin 9 (HP3DC2TR):** INT2
- Pin 3 (AL003DC2A00) to Pin 6 (HP3DC2TR):** SDO
- Pin 4 (AL003DC2A00) to Pin 7 (HP3DC2TR):** SDA
- Pin 5 (AL003DC2A00) to Pin 8 (HP3DC2TR):** SCL
- Pin 6 (AL003DC2A00) to Pin 1 (HP3DC2TR):** CS
- Pin 7 (AL003DC2A00) to Pin 2 (HP3DC2TR):** CS
- Pin 8 (AL003DC2A00) to Pin 3 (HP3DC2TR):** CS
- Pin 9 (AL003DC2A00) to Pin 4 (HP3DC2TR):** CS
- Pin 10 (AL003DC2A00) to Pin 5 (HP3DC2TR):** CS
- Pin 11 (AL003DC2A00) to Pin 6 (HP3DC2TR):** CS
- Pin 12 (AL003DC2A00) to Pin 7 (HP3DC2TR):** CS
- Pin 13 (AL003DC2A00) to Pin 8 (HP3DC2TR):** CS
- Pin 14 (AL003DC2A00) to Pin 9 (HP3DC2TR):** CS

The HP3DC2TR module is also connected to a 3V3_WLAN_P supply via a 0.6 ohm resistor (R183). The AL003DC2A00 module is connected to a 3V3_WLAN_P supply via a 0.6 ohm resistor (R183). The AL003DC2A00 module is also connected to a 3V3_WLAN_P supply via a 0.6 ohm resistor (R183). The AL003DC2A00 module is also connected to a 3V3_WLAN_P supply via a 0.6 ohm resistor (R183).

Green CLK Circuitry



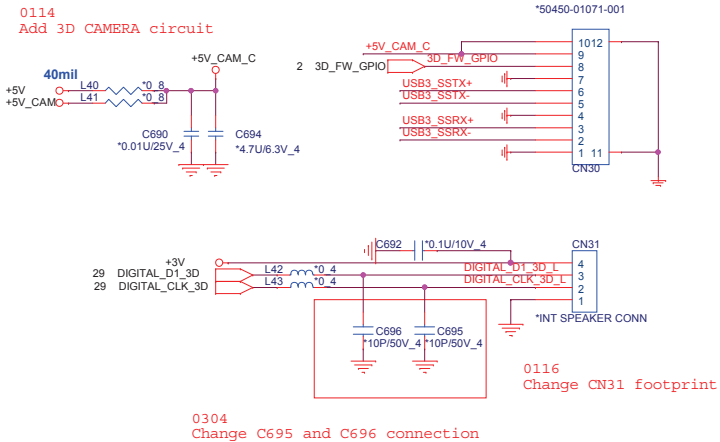
Change pin11 power to +3V_AON...GC6 2.0



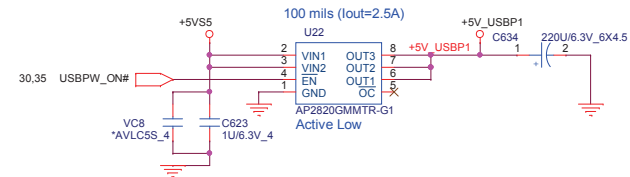
PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 32 -- TPM/G-Sensor/G-CLK/TS/FP	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 32 of	49

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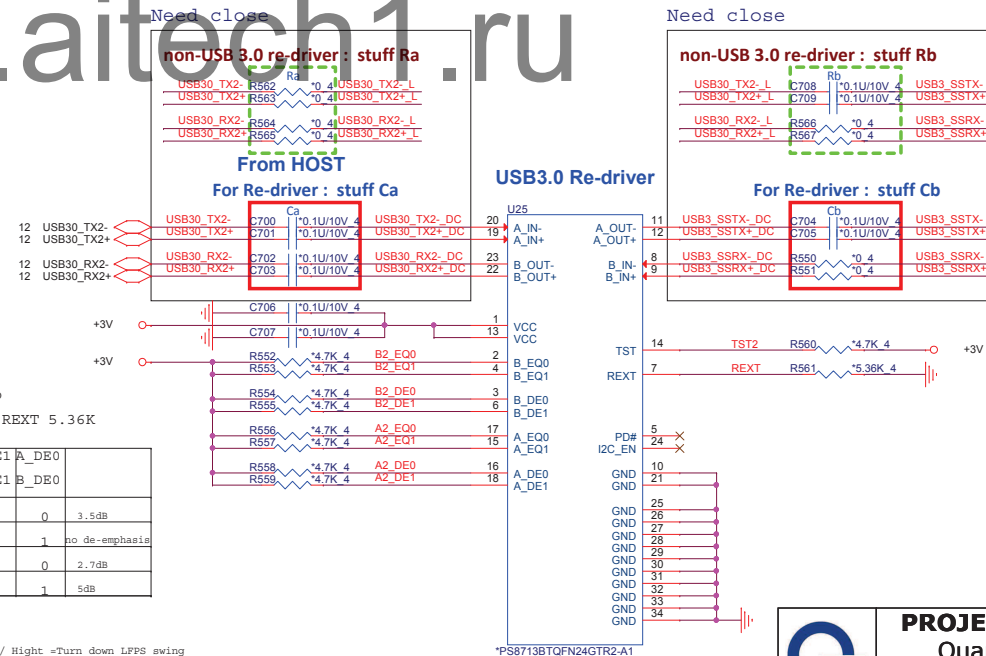
0216
Change CN11
from DFHS09FR596
to DFHS09FR613



Need close


non-USB 3.0 re-driver: stuff Ra

USB30 TX2, RX2 Ra USB30 TX2, I

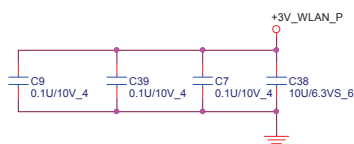
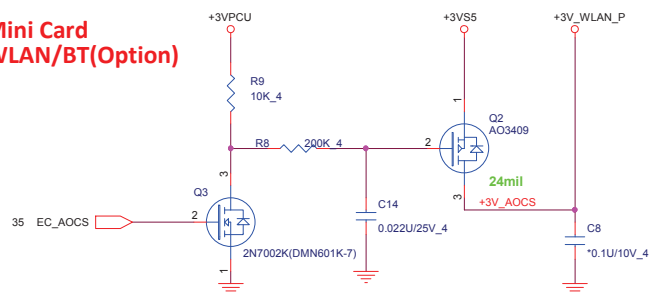


A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

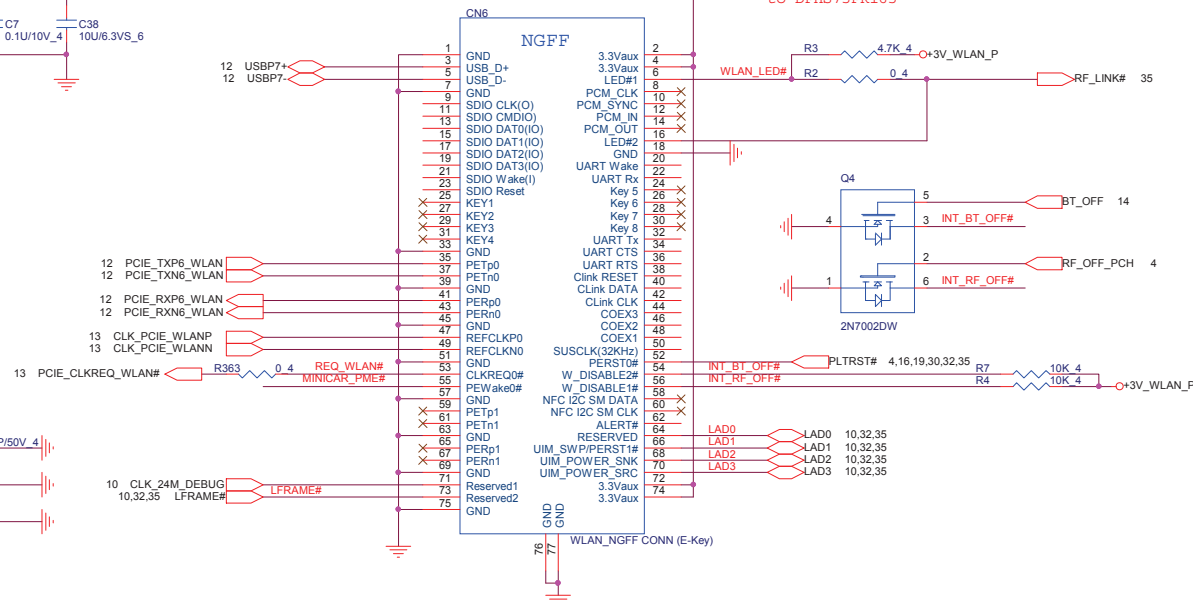
	PROJECT :Y11X-6L Quanta Computer Inc.		
	Size Custom	Document Number 33 – USB3.0/EMI CAP/3D CAM	Rev 1A
	Date: Wednesday, May 06, 2015	Sheet	33 of 49

Mini Card WLAN/BT(Optional)

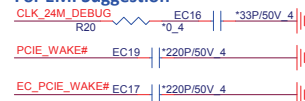


0216
Change CN6
from DFHS75FR127
to DFHS75FR092

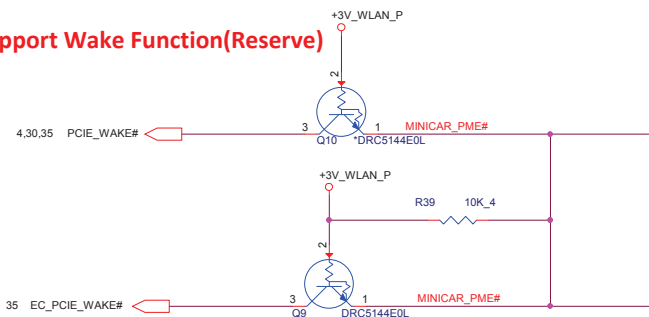
0323
Change CN6
from DFHS75FR092
to DFHS75FR165



For EMI Suggestion

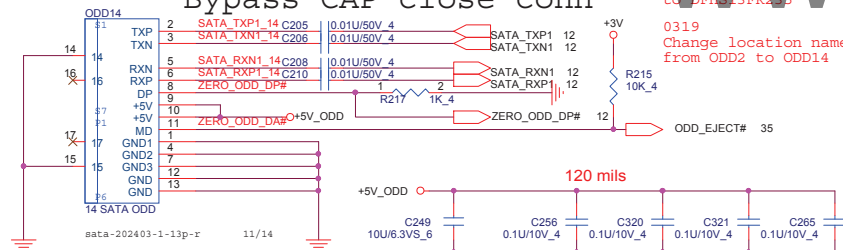


Support Wake Function(Reserve)

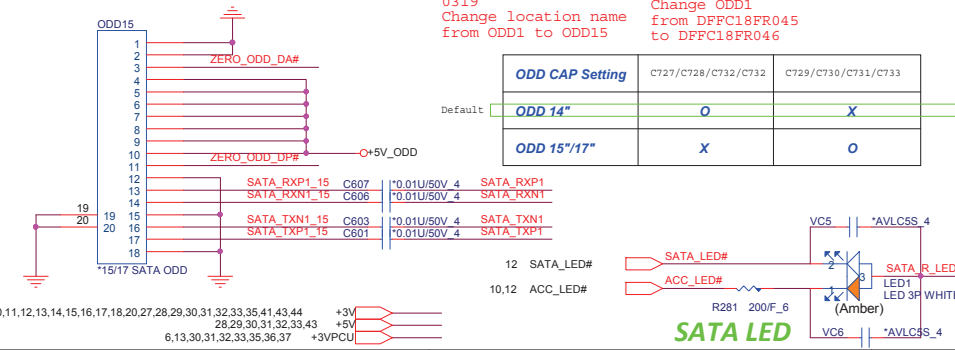


14" SATA ODD

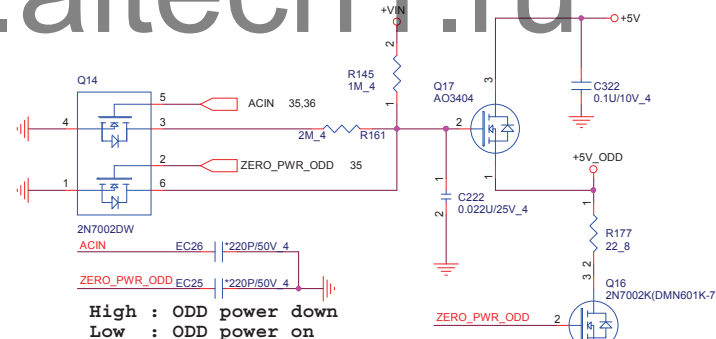
Bypass CAP close conn



15/17" SATA ODD



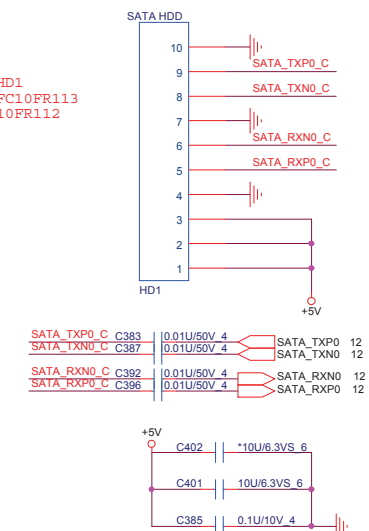
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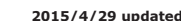


High : ODD power down
Low : ODD power on

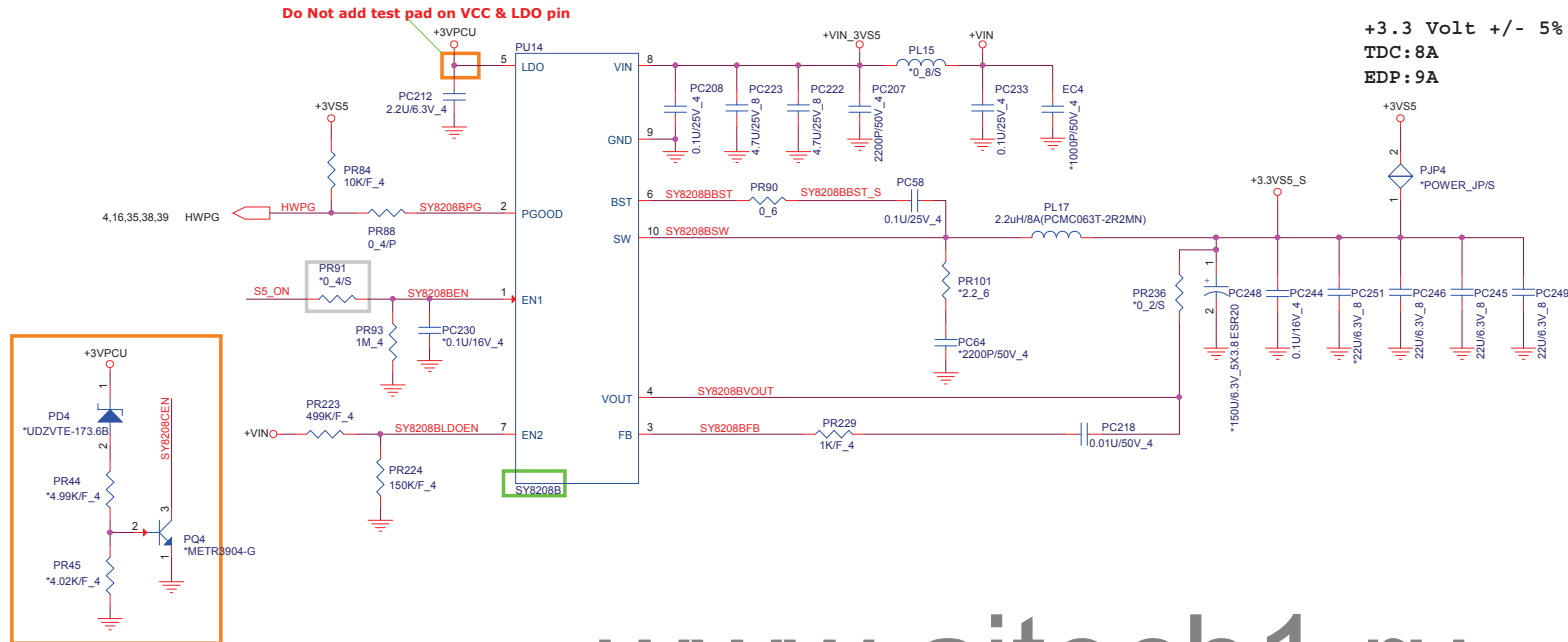
HDD

0216
Change HD1
from DFPC10FR113
to DFPC10FR112



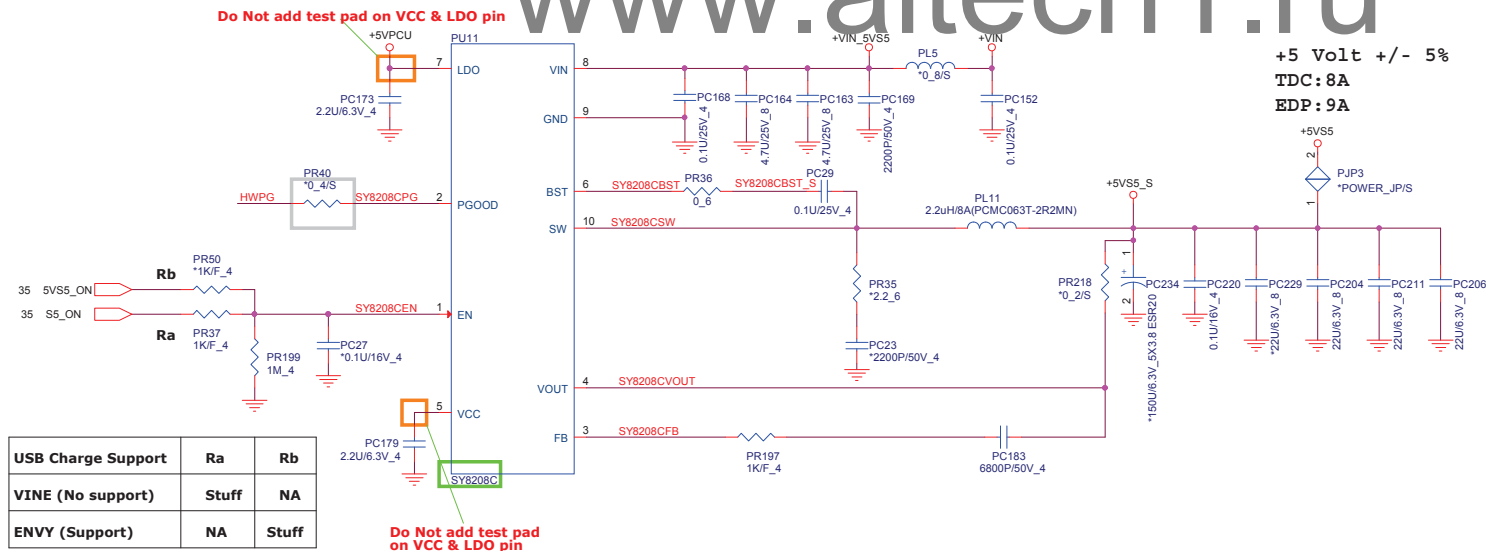


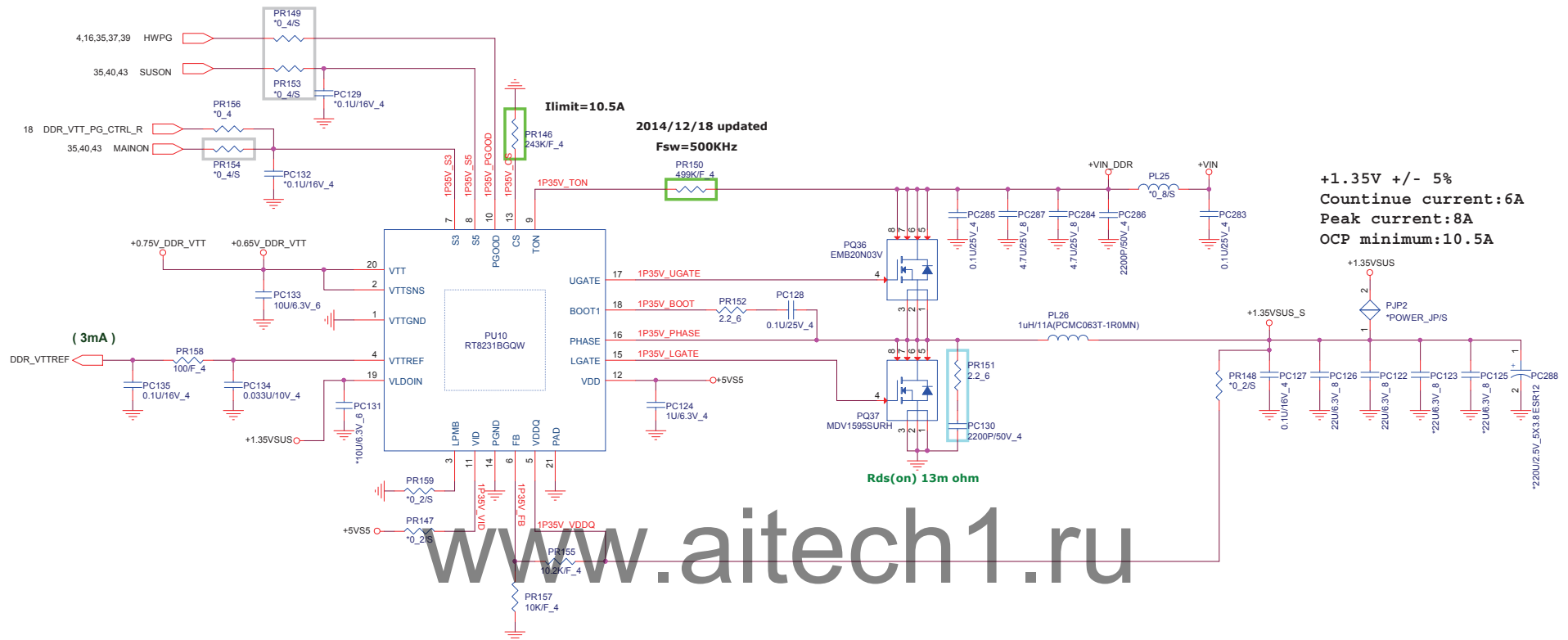
Size Custom	Document Number Charger (BQ24780)	Rev 1A
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2014/12/18 updated

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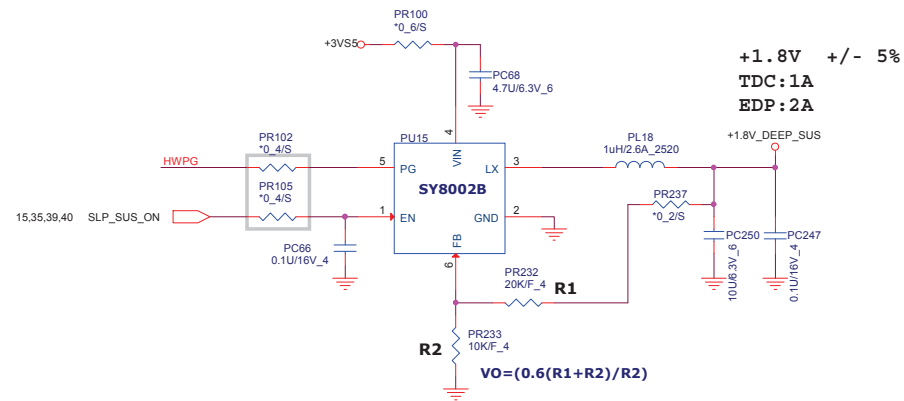
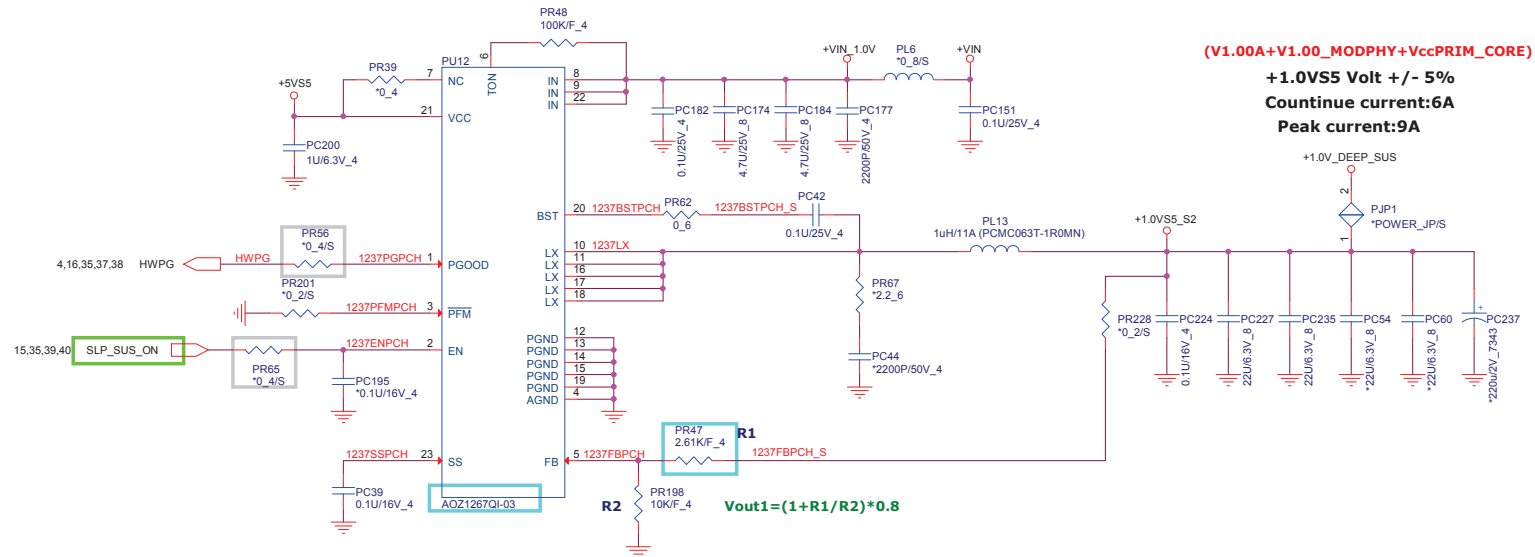





+VIN 28,31,33,34,36,37,39,41,42,43,44,45,46
+5VS5 4,30,32,33,37,39,40,41,42,43,44,45,46
+0.65V_DDR_VTT 17,18
+1.35VSUS 3,6,17,18,40,46

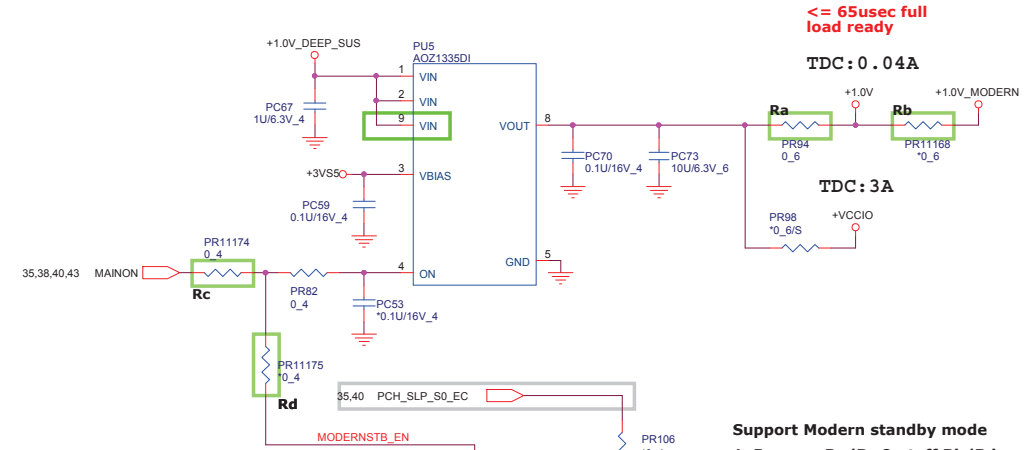
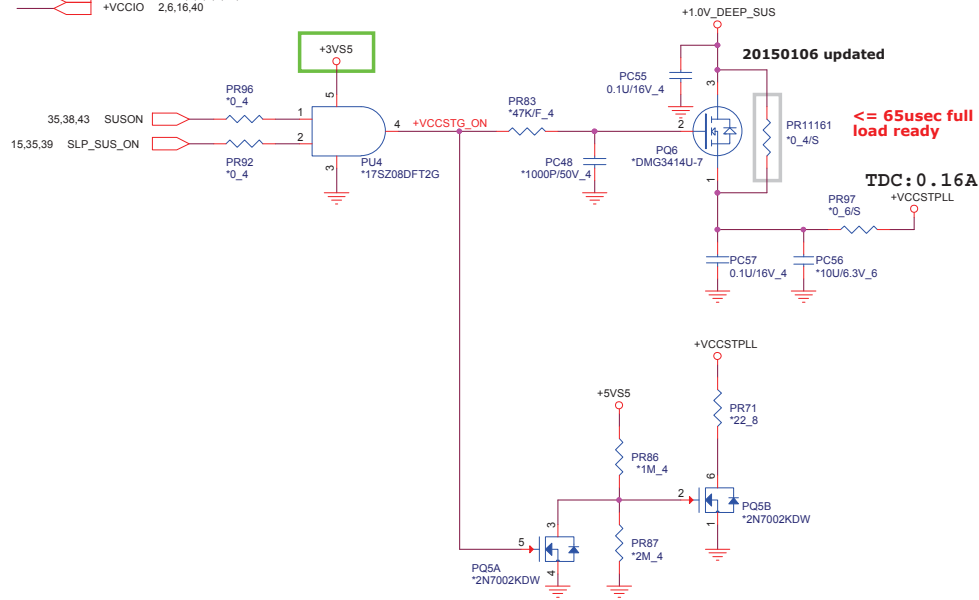
	PROJECT :Y11X-6L	
	Quanta Computer Inc.	
Size Custom	Document Number DDR3 (RT8231B)	Rev 1A
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+VIN 28,31,33,34,36,37,38,41,42,43,44,45,46
 +5VS5 4,30,32,33,37,38,40,41,42,43,44,45,46
 +3VS5 4,10,15,16,32,34,35,37,40,43,46
 +1.8V_DEEP_SUS 9,15
 +1.0V_DEEP_SUS 9,13,15,16,40



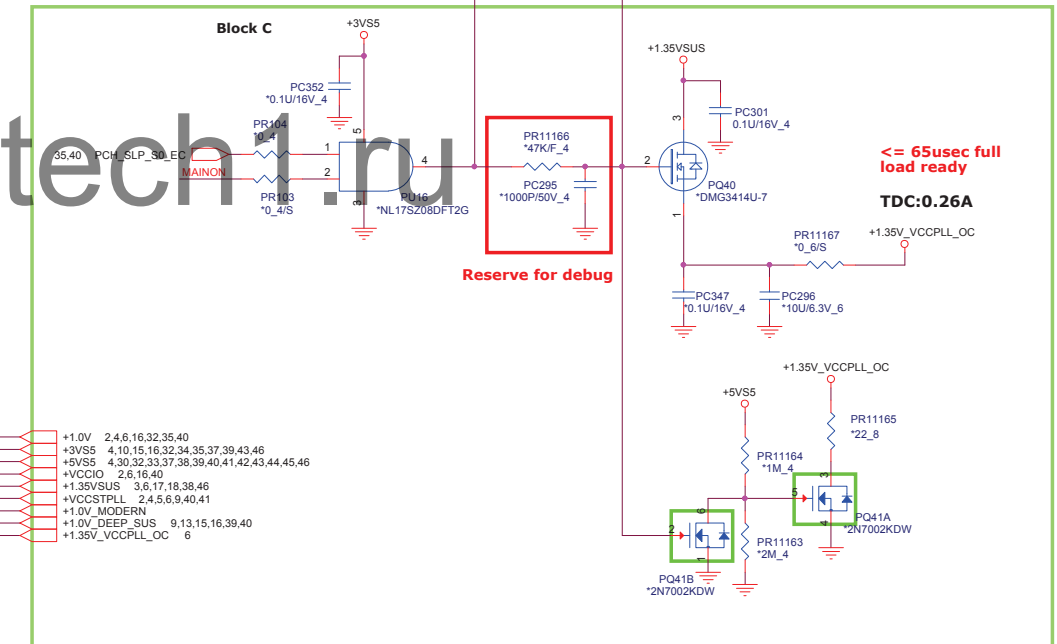
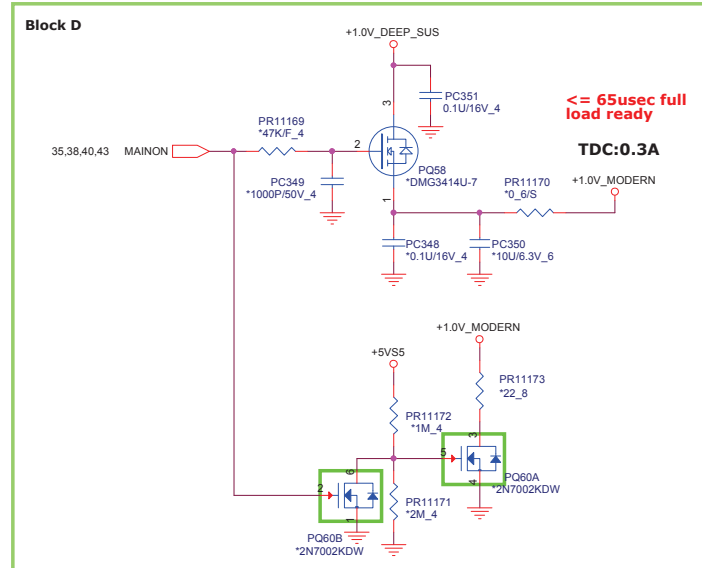


+1.0V_DEEP_SUS 9,13,15,16,39,40
 +1.0V 2,4,6,16,32,35,40
 +5VS5 4,30,32,33,37,38,39,40,41,42,43,44,45,46
 +VCCSTPLL 2,4,5,6,9,40,41
 +VCCIO 2,6,16,40



- Support Modern standby mode**
1. Remove Ra/Rc & stuff Rb/Rd
 2. stuff block C & D

Reserve for Modern StandBy

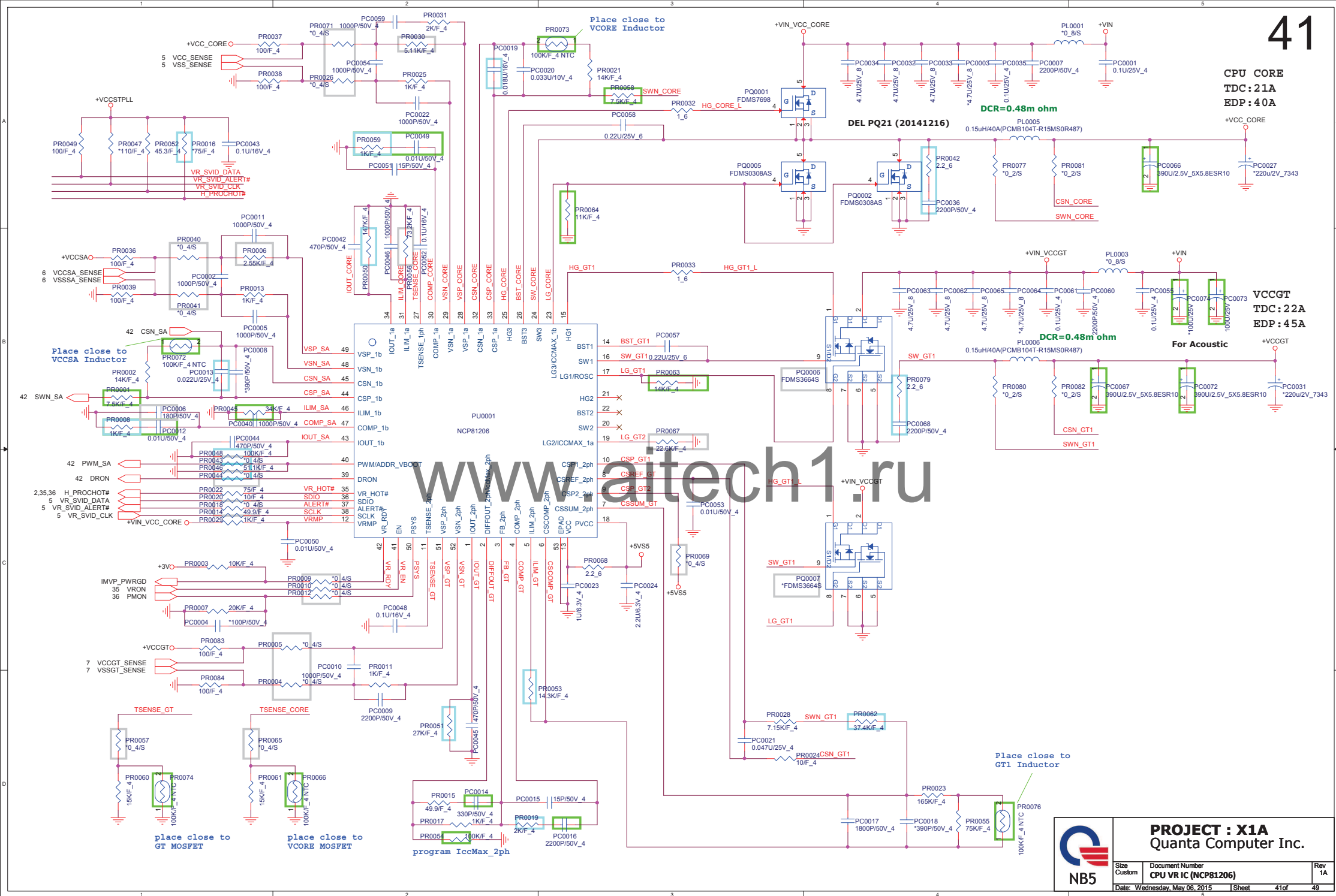


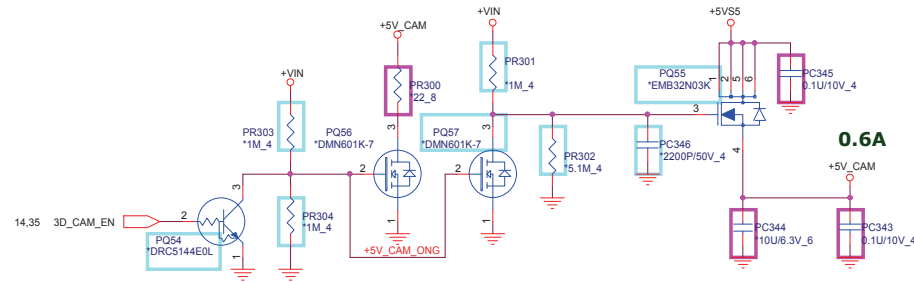
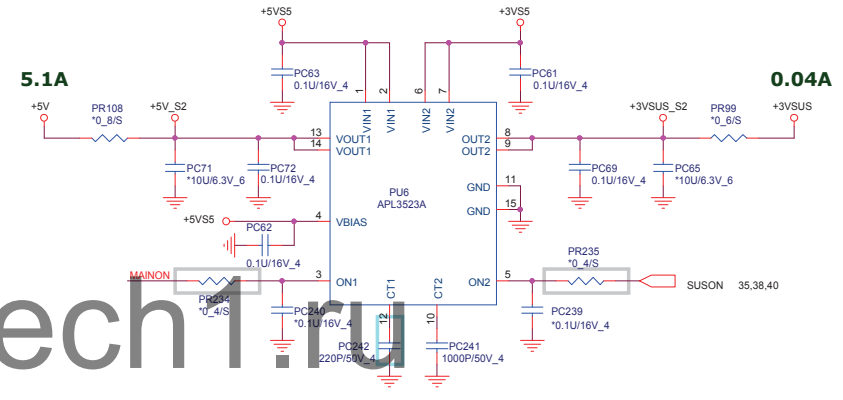
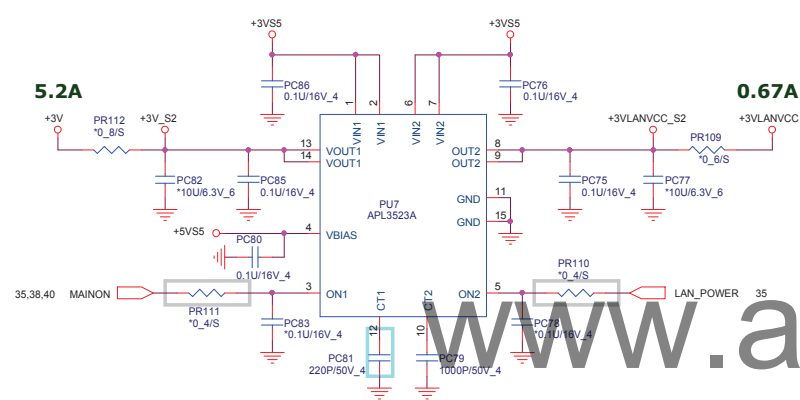
Reserve for debug

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+1.0V    2,4,6,16,32,35,40
+3VSUS   4,10,15,16,32,34,35,37,39,43,46
+5VSUS   4,30,32,33,37,38,39,40,41,42,43,44,45,46
+VCCIO   2,6,16,40
+1.35VSUS 3,6,17,18,38,46
+VCCSTPLL 2,5,6,9,40,41
+1.0V_MODERN
+1.0V_DEEP_SLEEP 9,13,15,16,39,40
+1.35V_VCCPLL_OC 6

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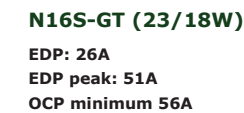


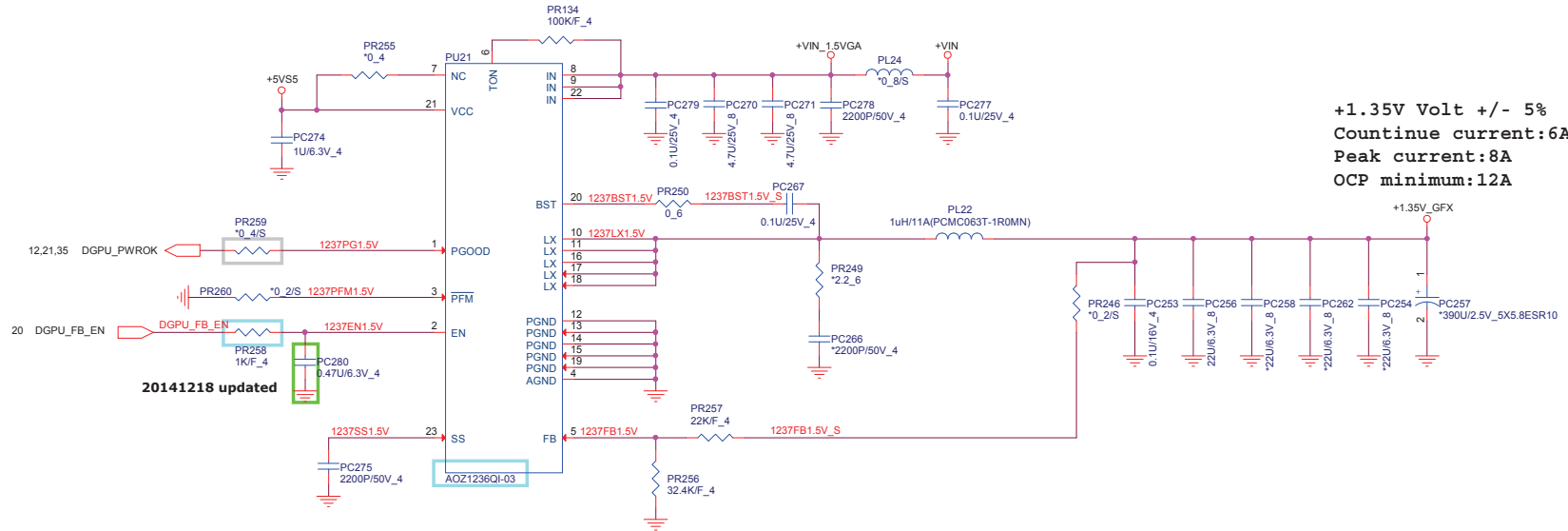
2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,44 +3V
28,29,30,31,32,33,34 +5V
28,31,33,34,36,37,38,39,41,42,44,45,46 +VIN
4,10,15,16,32,34,35,37,39,40,46 +3VS5
4,30,32,33,37,38,39,40,41,42,44,45,46 +5VS5
30,32 +3VLANVCC



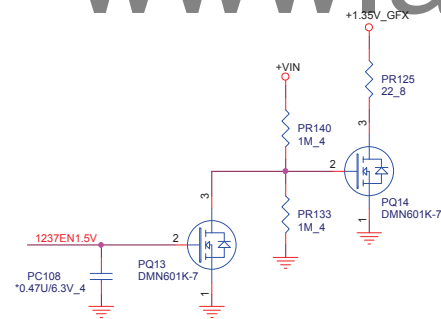
PROJECT :Y11X-6L
Quanta Computer Inc.

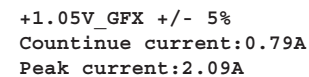
Size Custom	Document Number Load switch IC (APL3523A)	Rev 1A
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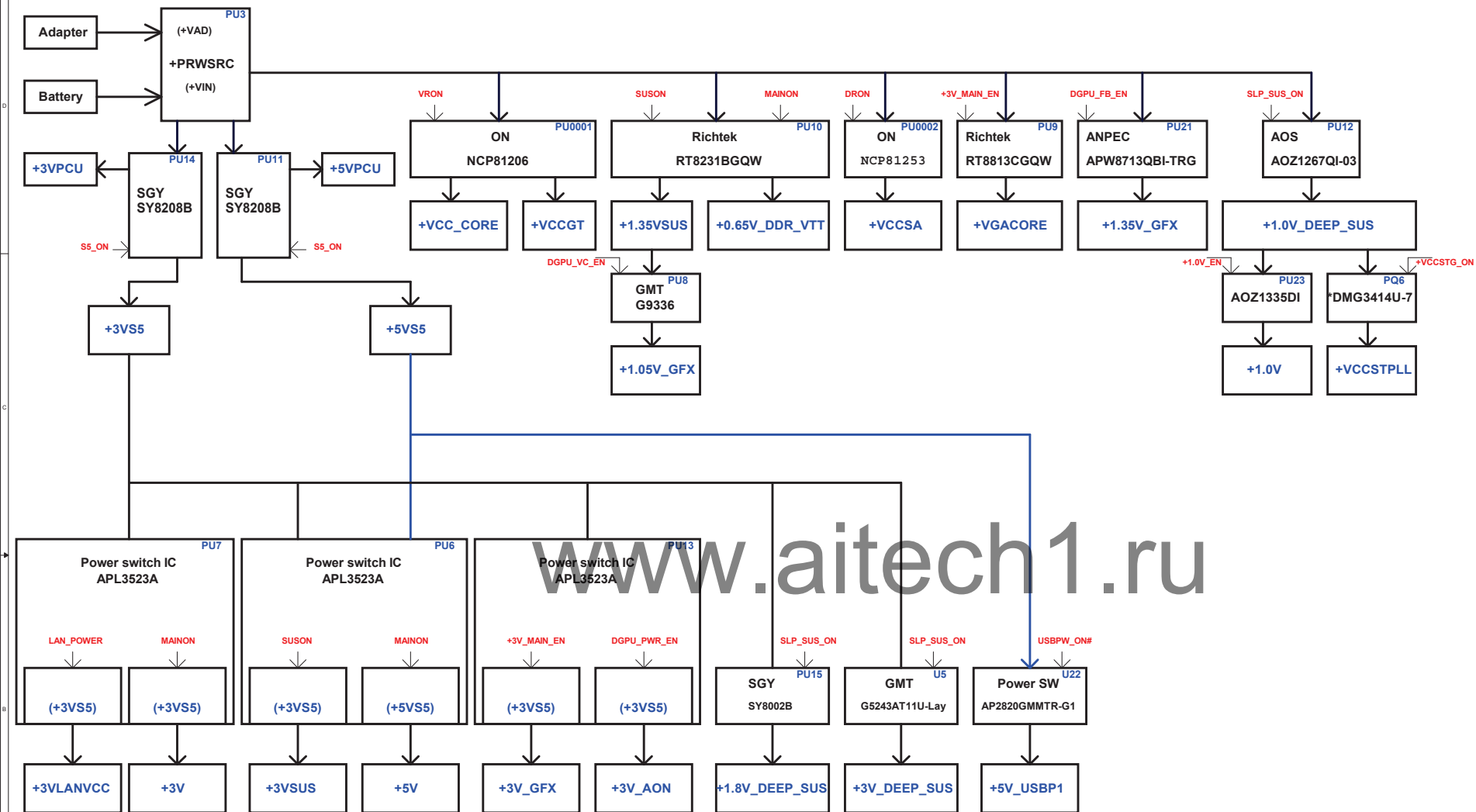


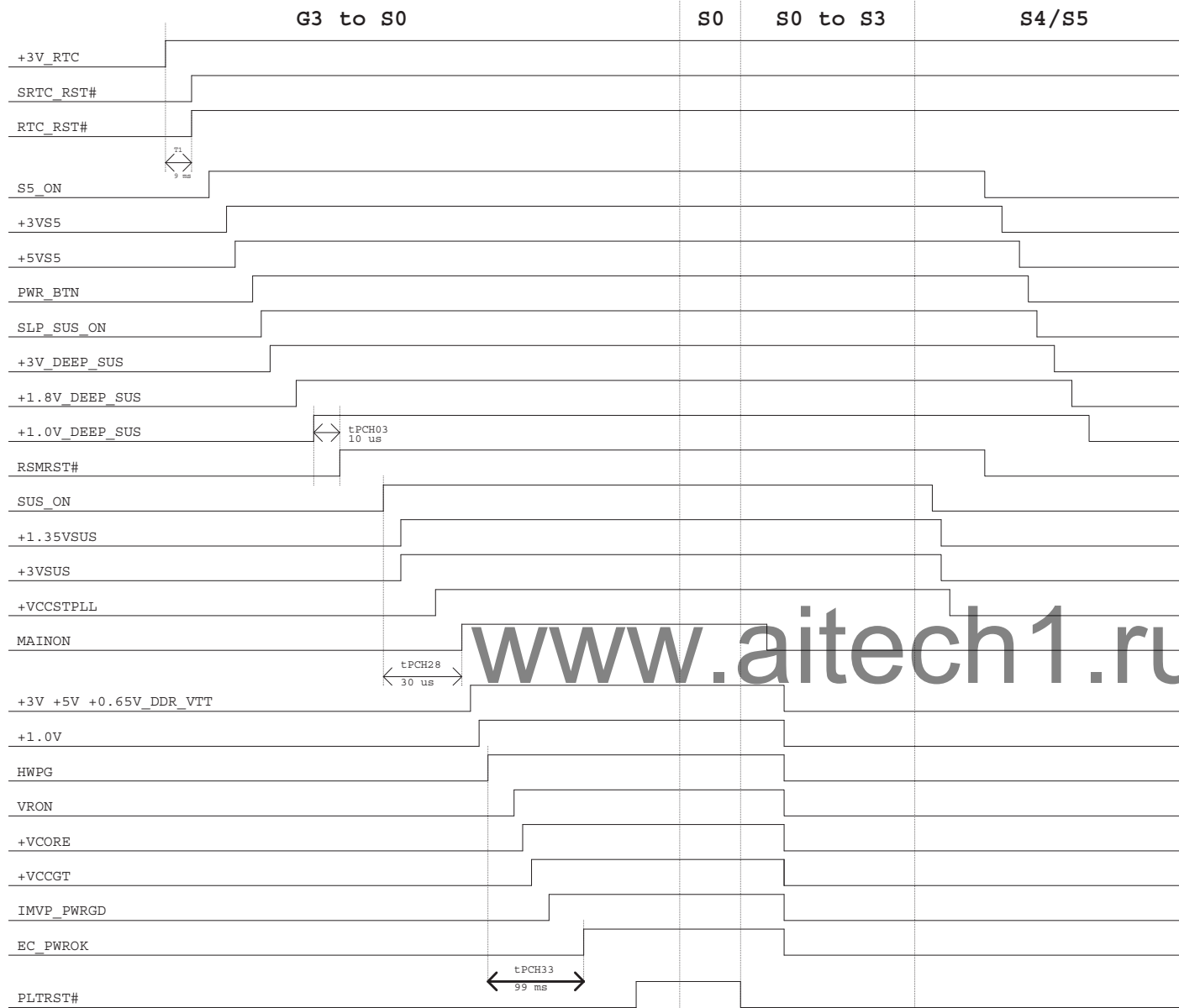
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